

## R03/V03 UMA BLOCK DIAGRAM

LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : GND  
LAYER 6 : BOT

DDRIII-SODIMM1  
A 00  
PAGE 16

DDRIII 1333 MT/s

DDRIII-SODIMM2  
A 01  
PAGE 17

DDRIII 1333 MT/s

CPU  
Sandy Bridge 45W  
PGA 989

PAGE 4~8

FDI LINK  
2.5GT /s

DMI LINK  
2.5GT /s

INT HDMI

INT Dual CHANNEL LVDS

HDMI Switch

PAGE 19

HDMI CONN

PAGE 19

LCD CONN

1600 x 900 (HD) PAGE 18

Re-Driver  
SN75LVCP412RTJR  
PAGE 20

E-SATA  
PAGE 20

SATA4 300MB /S

SATA -HDD  
PAGE 21

SATA0 300MB /S

ODD  
PAGE 21

SATA1 300MB /S

3-axis Fall Sensor  
PAGE 21

SMBUS

Mobile Intel  
Series 6 Chipset

PCH

HM67  
Couger Point

BGA 989  
25 mm X 25 mm

PAGE 9~15

iGFX Interfaces

USB2.0

USB[0]

USB[11]

USB[8]

USB[10]

USB[12]

USB[8]

Express Card

R5538D001 PAGE 02

EXP Board

LED Board

PB Board

TP Board

HotKey Board

Keyboard Conn.  
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Touch Pad  
PAGE 28

LED  
PAGE 29

KBC  
ITE 8518

PAGE 23

PWM FAN  
& Thermal  
PAGE 31

SPI ROM  
512kB  
PAGE 27

SPI  
PAGE 27

SPI ROM  
4MB

25MHz

32.768KHz

IHDA

Audio Codec  
ALC 269Q-VB6-GR  
PAGE 25

Subwoofer  
MAX9759ETE  
PAGE 26

Speaker  
PAGE 25

Jack  
X2 PAGE 25

Digital-MIC  
PAGE 25

CRT Board  
PAGE 03

USB[4]

USB[5]

PCIE[3]

WLAN  
PAGE 05

WiMAX  
PAGE 04

USB3.0 Controller  
PAGE 06

PCIE[1]

PCIE[2]

PCIE[5]

BlueTooth  
PAGE 05

USB3.0 Ports x2  
PAGE 07

LAN  
Realtek  
RTL8111E-VB-GR  
PAGE 09

USB[6]

RJ45  
PAGE 10

USB Port x1  
PAGE 08

USB[2]

Charger  
PAGE 35

3/5V  
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1.5V\_SUS/0.75V\_DDR  
PAGE 37

Batt/DC-IN  
PAGE 34

1.05V\_PCH  
PAGE 38

VCCSA  
PAGE 39

CPU\_CORE  
PAGE 40

1.8V\_RUN  
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Size Document Number

Rev 2A

BLOCK DIAGRAM

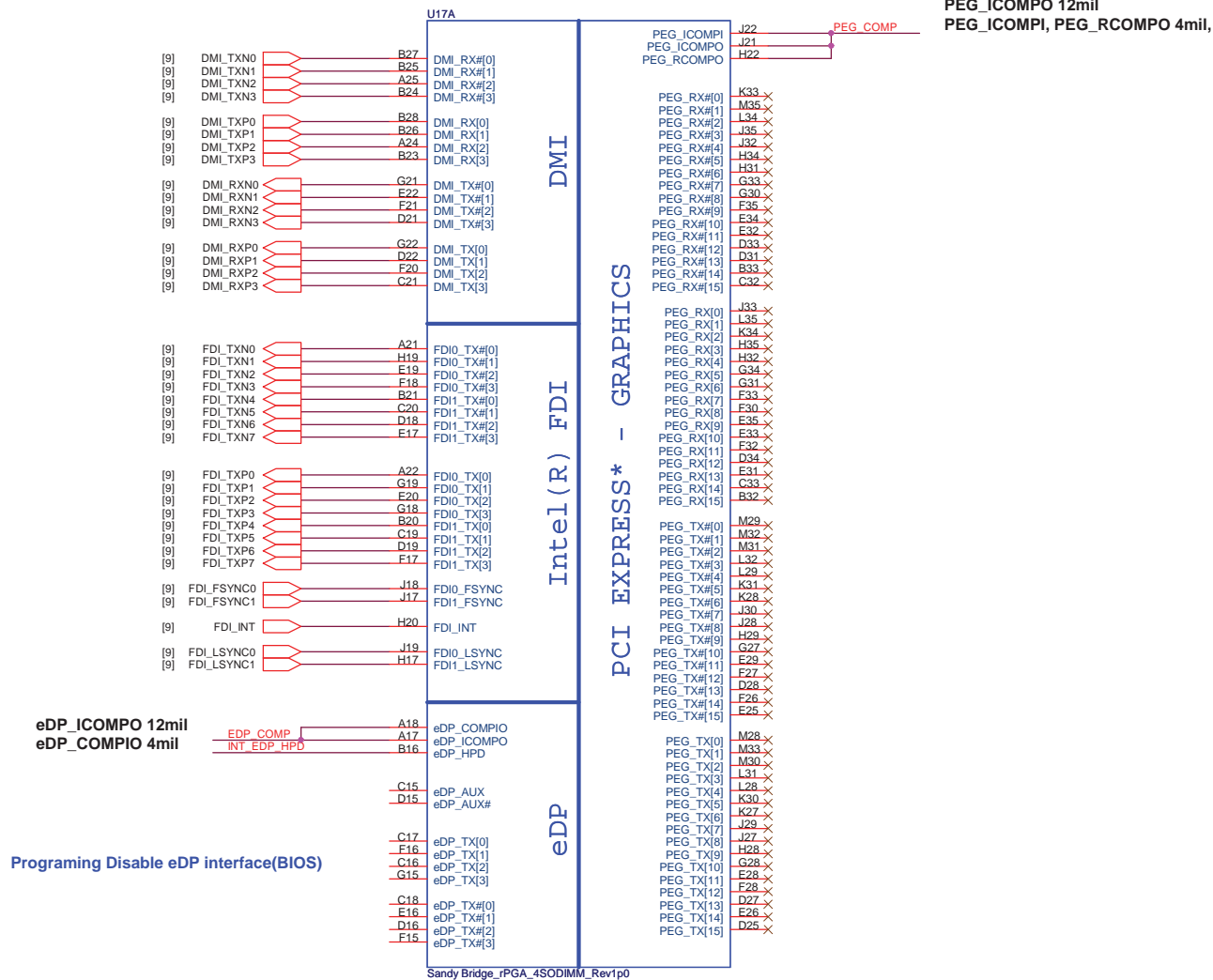
Date: Wednesday, October 06, 2010 Sheet 1 of 42

| power<br>State | +RTC_CELL | +DC_IN<br>+DC_IN_SS<br>+PWR_SRC<br>+5V_ALW_2<br>+3.3V_ALW<br>+5V_ALW<br>+15V_ALW<br>+3.3V_LAN (for V03) | +VCHGR<br>+PWR_SRC<br>+5V_ALW_2<br>+3.3V_ALW<br>+5V_ALW<br>+15V_ALW<br>+3.3V_LAN (for V03) | +5V_SUS<br>+3.3V_SUS<br>+1.5V_SUS<br>+1.5V_CPU<br>+DDR_VTTREF<br>+3.3V_LAN (for R03) | +VCC_CORE<br>+1.05V_PCH<br>+5V_RUN<br>+3.3V_RUN<br>+1.8V_RUN<br>+1.5V_RUN<br>+VCCSA<br>+0.75V_DDR_VTT<br>+LCDVCC<br>+VCC_GFX_CORE |  |
|----------------|-----------|---|--|--|---|--|
| S0             | ON        | ON  | ON   | ON   | ON  |  |
| S1             |           |   |  |  |   |  |
| S3             | ON        | ON  | ON   | ON   | OFF   |  |
| S4/S5 AC       | ON        | ON  |  |  |   |  |
| S4/S5 DC Only  | ON        |   | ON   | OFF  | OFF   |  |
| AC/DC No Exist | ON        | OFF   | OFF  | OFF  | OFF   |  |

|                            |  |  |  |  |  |  |  |  |
|----------------------------|--|--|--|--|--|--|--|--|
|                            |  |  |  |  |  |  |  |  |
| SMBCLK<br>SMBDATA          |  |  |  |  |  |  |  |  |
| SMB_CLK_ME1<br>SMB_DAT_ME1 |  |  |  |  |  |  |  |  |
| AB1A_CLK<br>AB1A_DATA      |  |  |  |  |  |  |  |  |

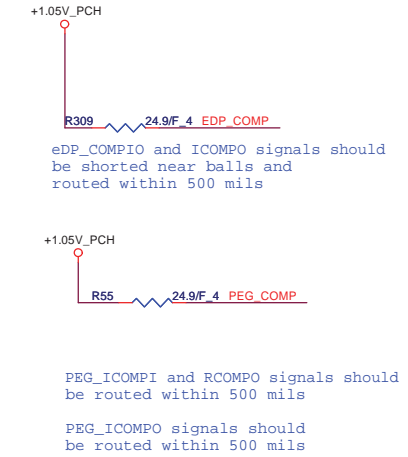


## Sandy Bridge Processor (DMI, PEG, FDI)

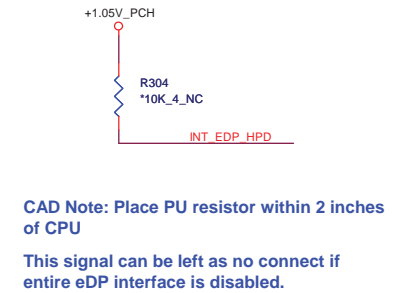


Programming Disable eDP interface(BIOS)

## DP &amp; PEG Compensation

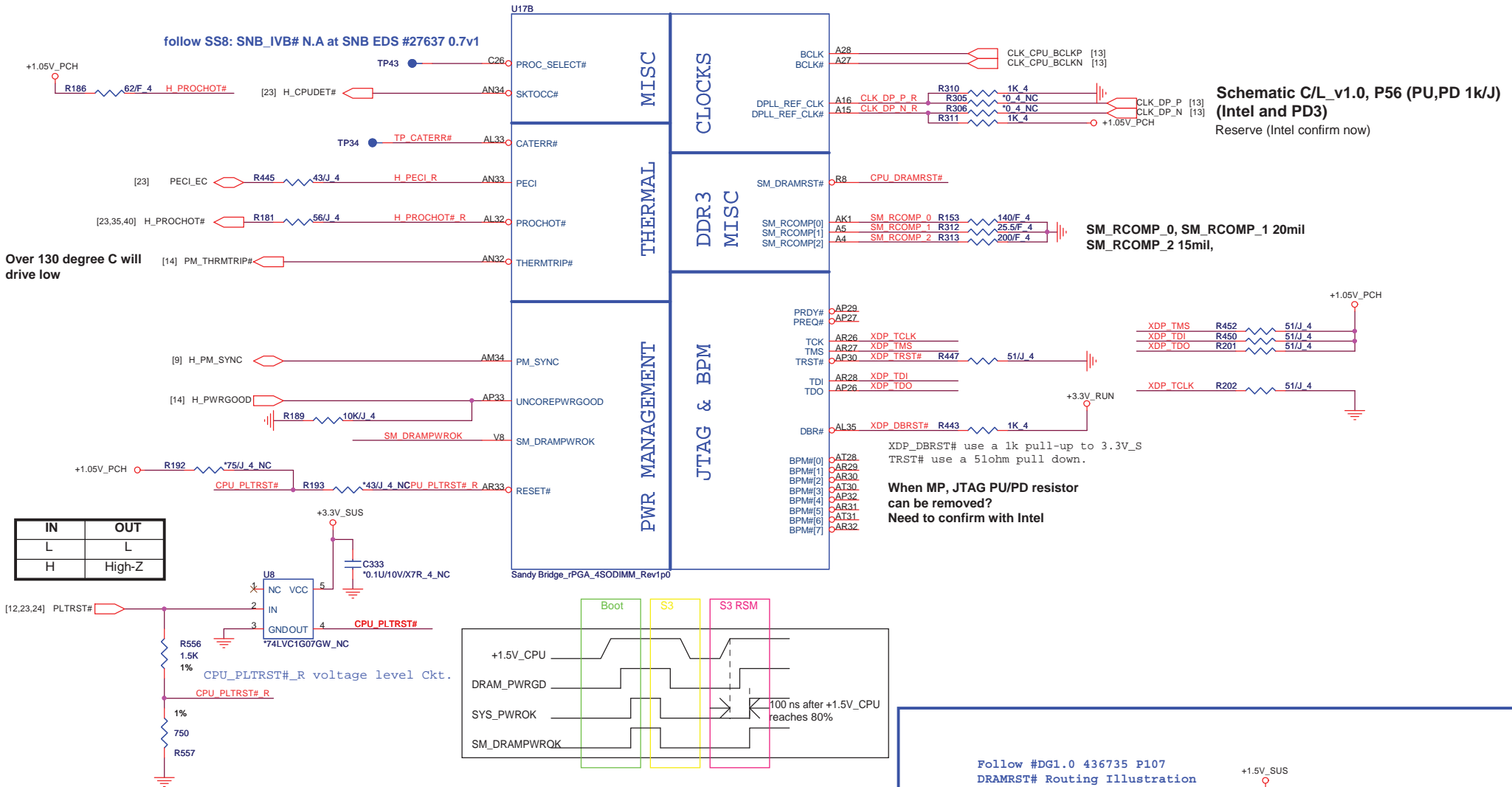


## eDP Hot-plug (Disable)



# Sandy Bridge Processor (CLK,MISC,JTAG)

follow SS8: SNB\_IVB# N.A at SNB EDS #27637 0.7v1



| IN | OUT    |
|----|--------|
| L  | L      |
| H  | High-Z |

| Pin1 | Pin2 | Pin4 |
|------|------|------|
| L    | L    | L    |
| L    | H    | L    |
| H    | L    | L    |
| H    | H    | H    |



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## POWER

**CPU Core Power**  
SNB 45W:95A  
470uF/4mohm x 4  
22uF x 16  
10uF x 10

**CPU VTT**  
SNB 45W:8.5A  
330uF/6mohm x 2  
22uF x 12  
22uF x 7 (Non-stuff)

**CPU VGT**  
SNB 45W:22A  
22uF x 12

## POWER

**SENSE LINES**  
VAXG\_SENSE  
VSSAXG\_SENSE

**VREF**  
SM\_VREF

**DDR3 - 1.5V RAILS**

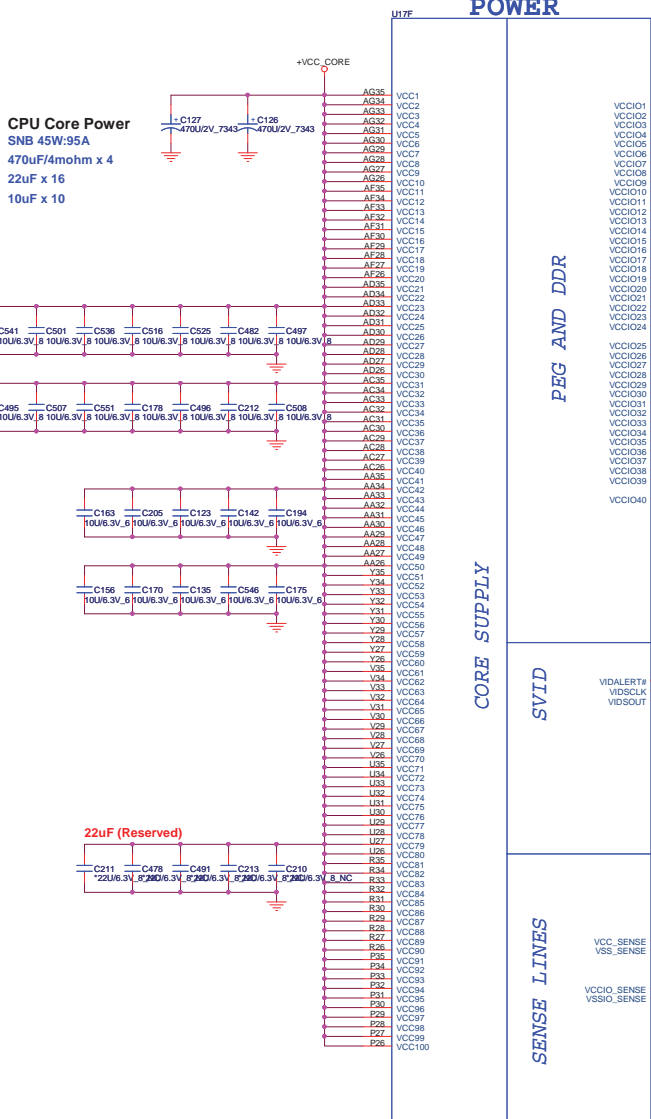
**SA RAIL**

**MISC**

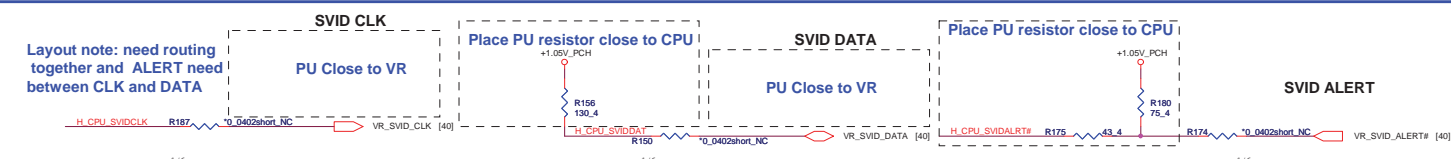
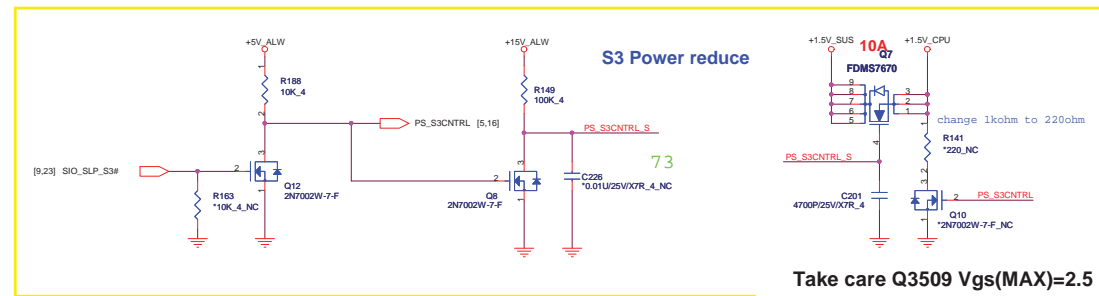
**1.8V RAIL**

**CPU MCH**  
SNB 45W: 5A  
330uF/6mohm x 1  
10uF x 6

**CPU SA**  
SNB 45W: 6A  
330uF/7mohm x 1  
10uF x 3



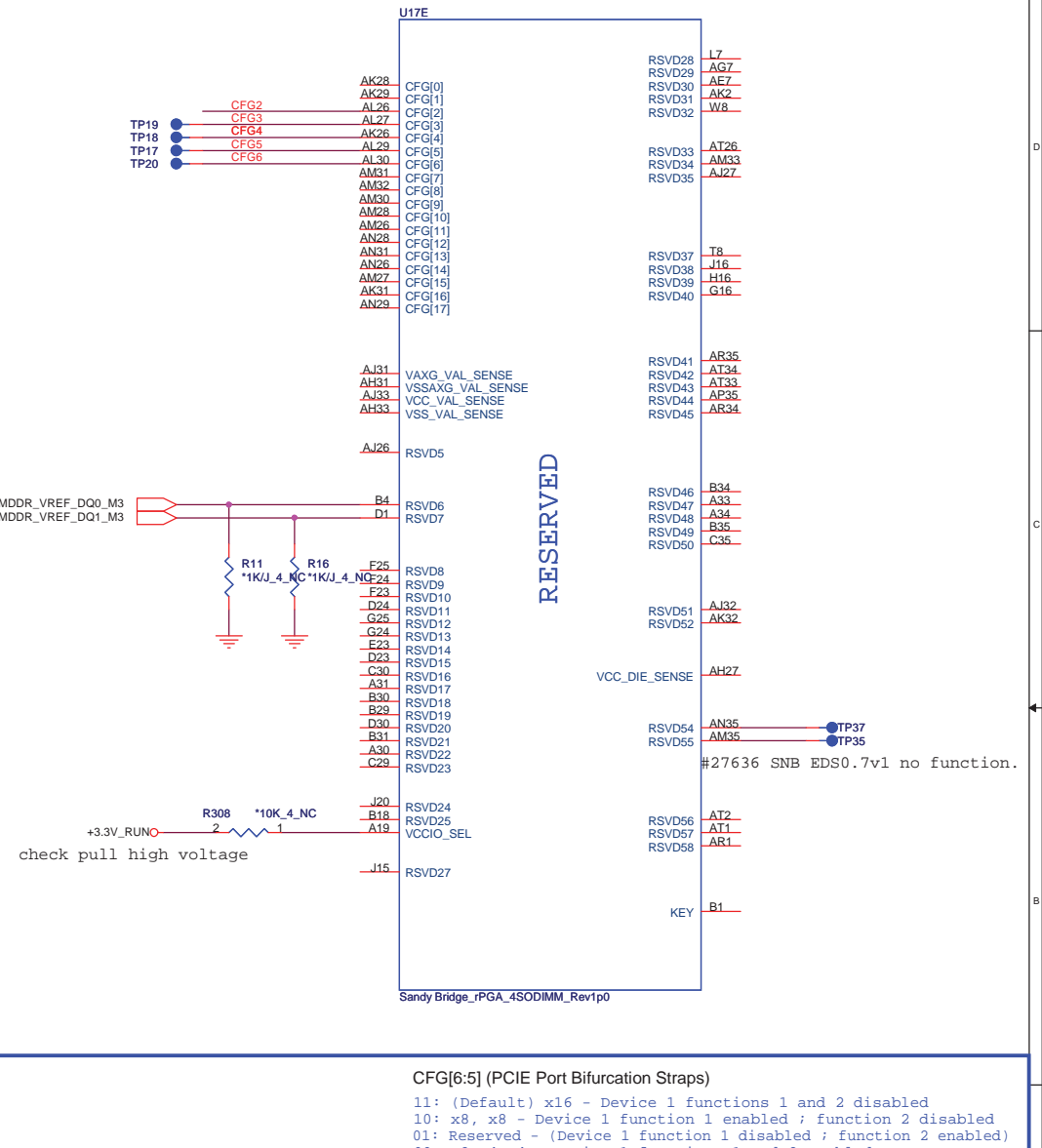
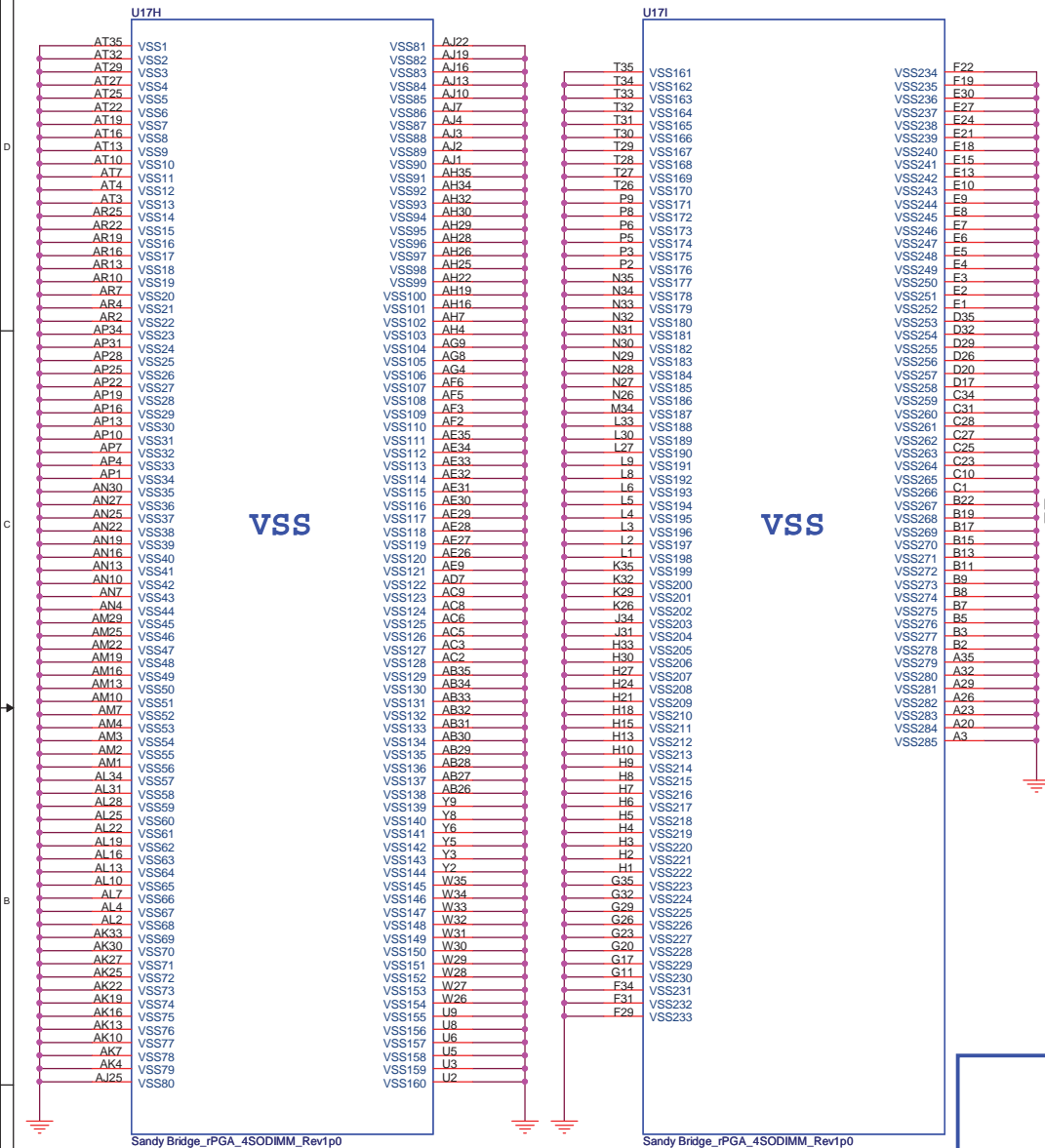
Change R8281,R8285, R8704,R8329 to +/-5%  
54.9 ohm has no 5%





## Sandy Bridge Processor (GND)

## Sandy Bridge Processor (RESERVED, CFG)



## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

|  | 1                                       | 0  |
|--|---|--|
| CFG2<br>(PCI-E Static x16 Lane Reversal) | Normal Operation                        | Lane Reversed                                |
| CFG3<br>(PCI-E Static x4 Lane Reversal)  | Normal Operation                        | Lane Reversed                                |
| CFG4<br>(DP Presence Strap)              | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |

CFG2 R199 1K/F 4



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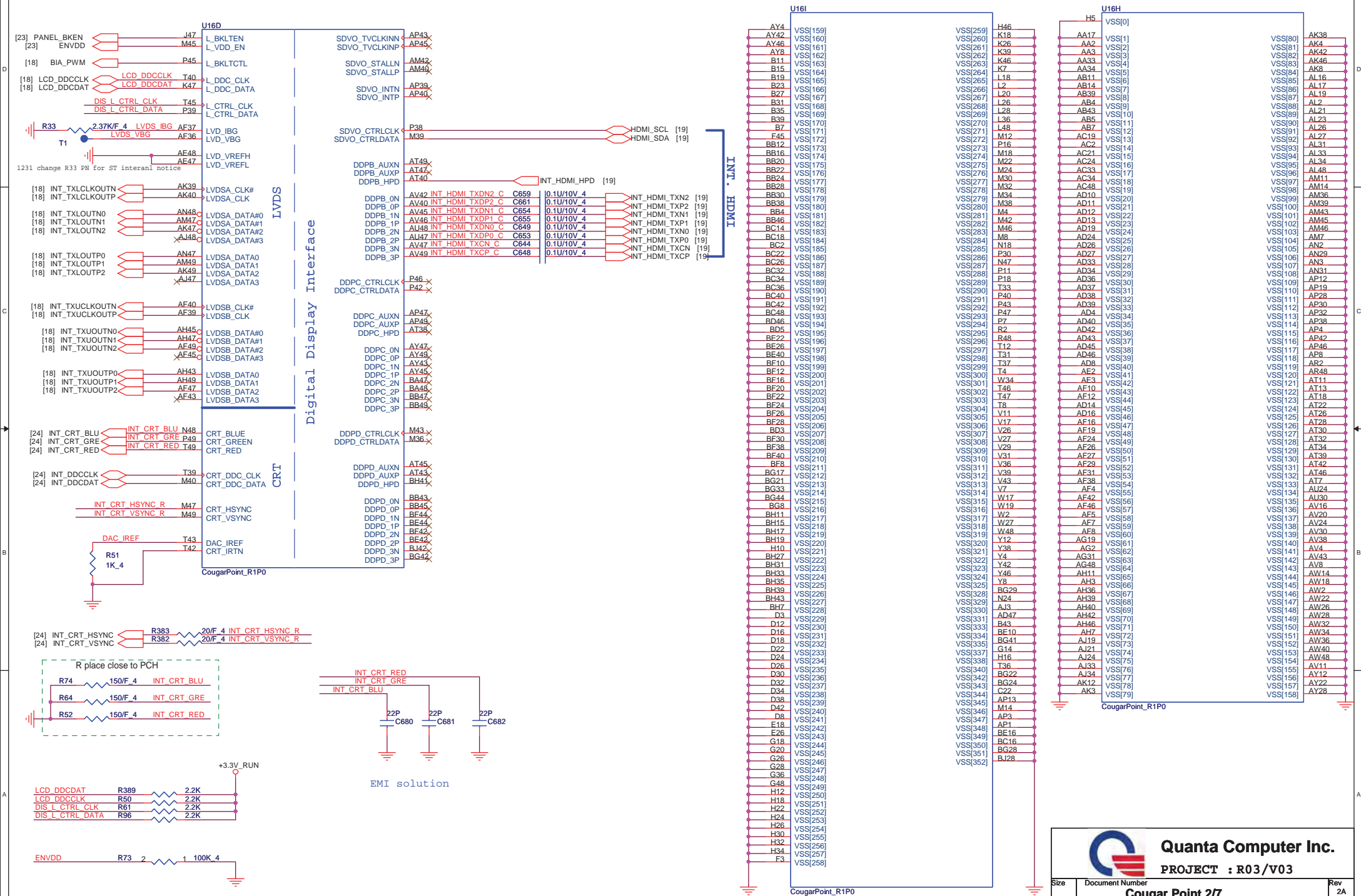
|      |                          |               |
|------|--------------------------|---------------|
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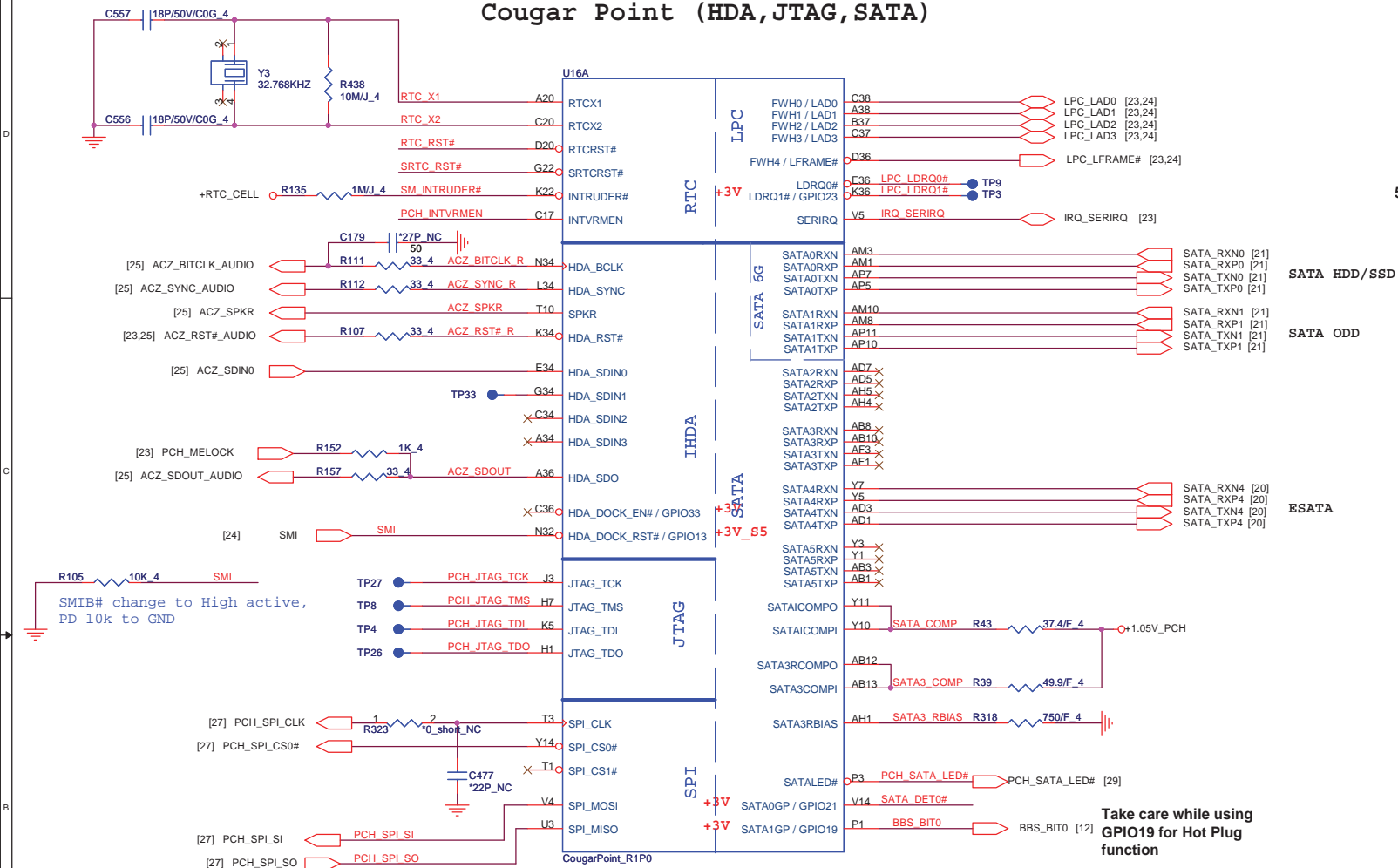


## Cougar Point (LVDS,DDI)

## Cougar Point (GND)

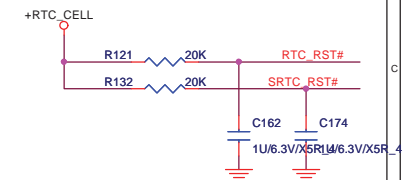
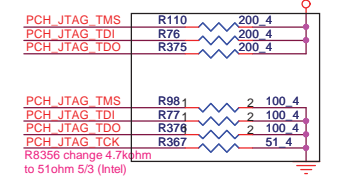


## Cougar Point (HDA, JTAG, SATA)



## PCH JTAG Debug (CLG)

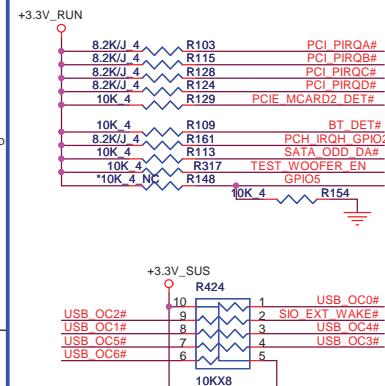
5% fine (Intel), 210-&gt;200 (PDDG, Intel) MP remove(Intel)



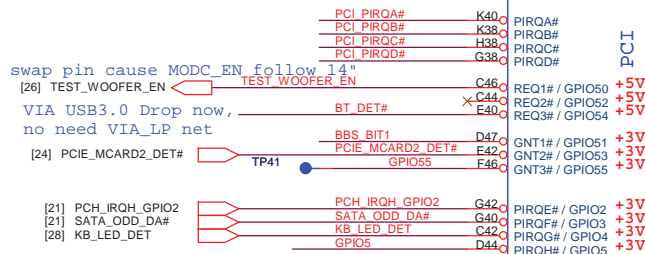
## PCH Strap Table

| Pin Name | Strap description            | Sampled | Configuration   | note                                 |
|----------|------------------------------|---------|---|--------------------------------------|
| SPKR     | No reboot mode setting       | PWROK   | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode | +3.3V_SUS R41 1K 4 NC ACZ_SPKR       |
| HDA_SDO  | Flash Descriptor Security    | PWROK   | 0 = Default (weak pull-down 20K)<br>1 = Override                  | +3.3V_SUS R146 1K 4 NC ACZ_SDOUT     |
| Del 0510 |                              |         | Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91                  |                                      |
| INTVRMEN | Integrated 1.05V VRM enable  | ALWAYS  | Should be always pull-up  | +RTC_CELL R434 330K/J 4 PCH_INTVRMEN |
| HDA_SYNC | On-Die PLL VR Volatge Select | RSMRST  | 0 = Support by 1.8V (weak PD)<br>1 = Support by 1.5V              | +3.3V_SUS R118 1K 4 ACZ_SYNC_R       |

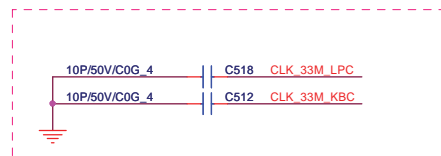
## PCI/USBOC# Pull-up(CLG)



## change SMIB# to SMI

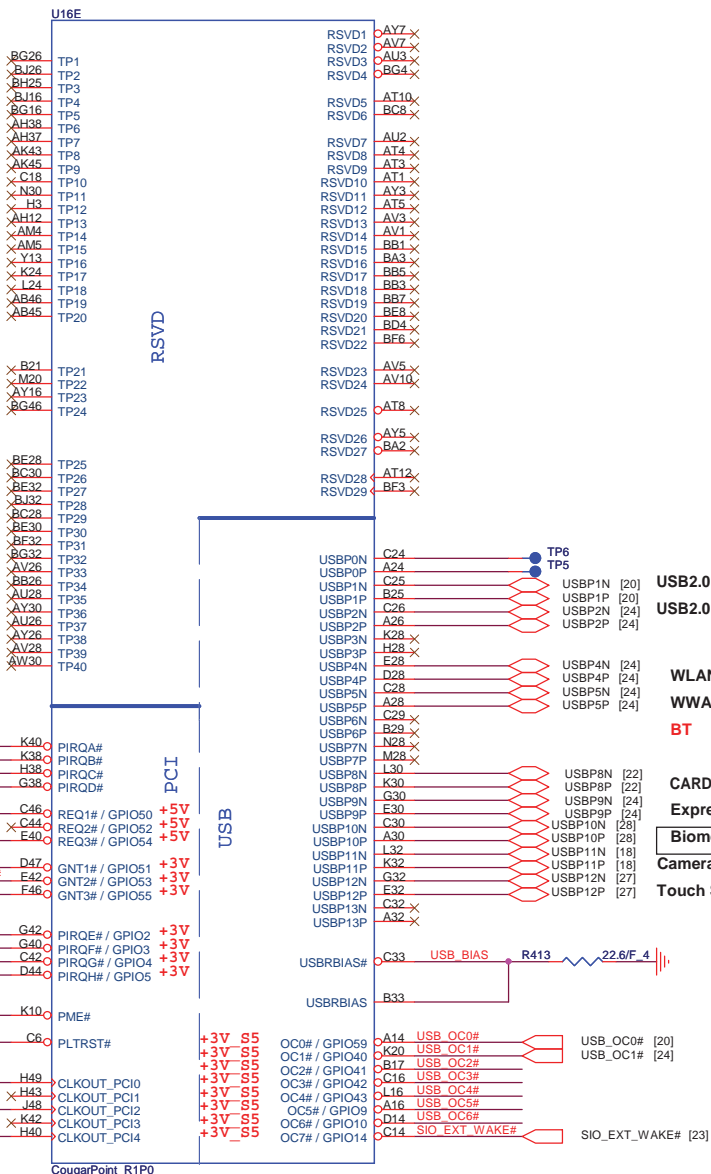


Check with BIOS program or not? (have to be not)



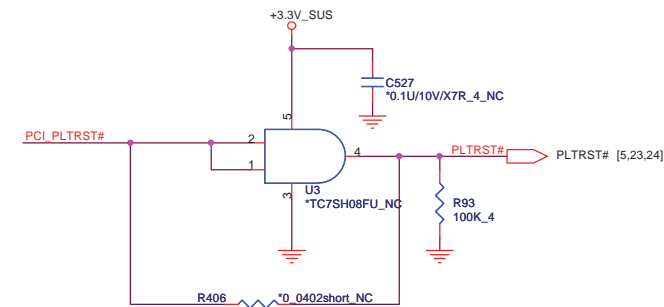
EMI solution pop C518, C512

## Cougar Point-M (PCI,USB,NVRAM)



|                         |
|-------------------------|
| SV_SET_UP               |
| High = Strong (Default) |

## PLTRST#(CLG)



## USB2.0 & ESATA LEFT USB2.0 RIGHT

## WLAN WWAN BT

## CARD READER Express card

## Biometric Camera

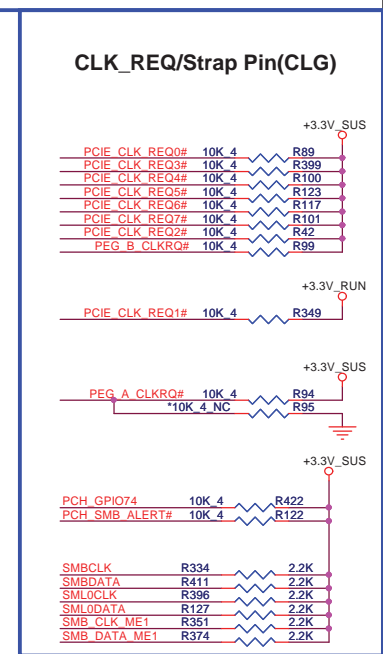
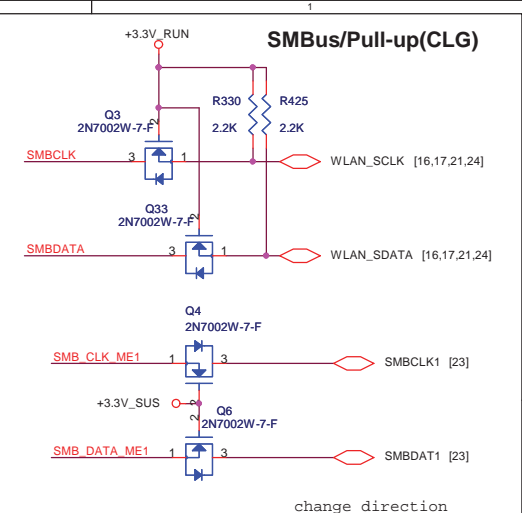
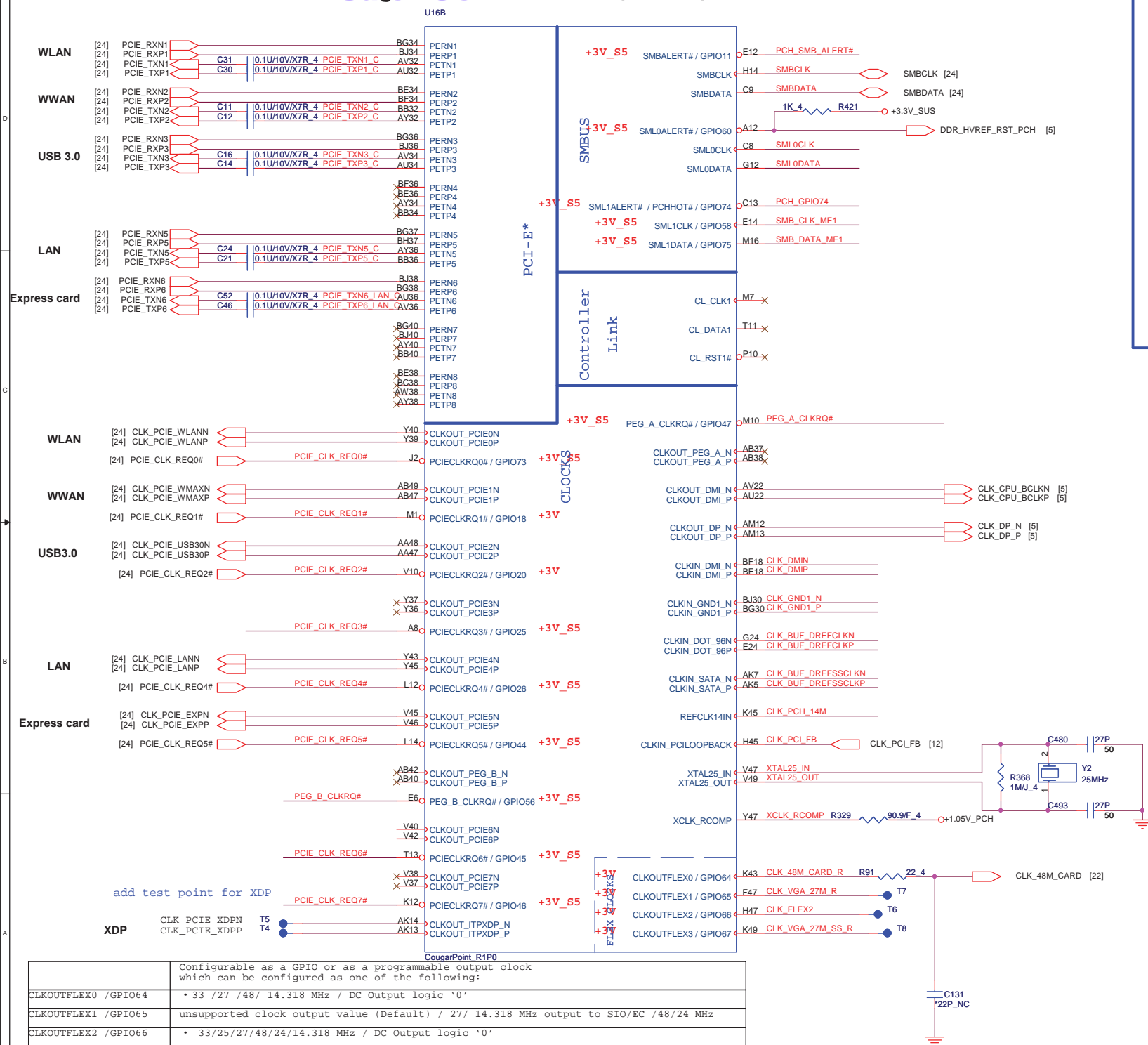
## Touch Screen

| Pin Name   | Strap description                     | Sampled       | Configuration  |       |       |               |   |   |       |   |   |     |
|--|---------------------------------------|---------------|--|-------|-------|---------------|---|---|-------|---|---|-----|
| GNT2# / GPIO53   | ESI strap (Server only)               | PWROK         | Should not be pull-down<br>(weak pull-up 20K)  |       |       |               |   |   |       |   |   |     |
| GNT3# / GPIO55   | Top-Block Swap Override               | PWROK         | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K)  |       |       |               |   |   |       |   |   |     |
| Defined in EDS (Intel)   |                                       |               |  |       |       |               |   |   |       |   |   |     |
| GNT1# / GPIO51   | Boot BIOS Selection 1 [bit-1]         | PWROK         | <table><tr><th>Bit 0</th><th>Bit 1</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table> | Bit 0 | Bit 1 | Boot Location | 1 | 1 | SPI * | 0 | 0 | LPC |
| Bit 0  | Bit 1                                 | Boot Location |  |       |       |               |   |   |       |   |   |     |
| 1  | 1                                     | SPI *         |  |       |       |               |   |   |       |   |   |     |
| 0  | 0                                     | LPC           |  |       |       |               |   |   |       |   |   |     |
| GPIO19   | Boot BIOS Selection 0 [bit-0]         | PWROK         |  |       |       |               |   |   |       |   |   |     |
| <div><div><div>BBS_BIT1</div><div>R102</div><div>*1K 4_NC</div></div><div><div>[11] BBS_BIT0</div><div>R327</div><div>*1K 4_NC</div></div></div> <div>Default weak pull-up on GNT0/1#<br/>[Need external pull-down for LPC BIOS]</div> |                                       |               |  |       |       |               |   |   |       |   |   |     |
| DF_TV5   | DMI and FDI Tx/Rx Termination Voltage | PWROK         | weak pull-down 20kohm  |       |       |               |   |   |       |   |   |     |
| <div><div><div>R314</div><div>2.2K</div><div>+1.8V_RUN</div></div><div><div>DF_TV5 [14]</div></div></div> <div>CheckList_1.0 p58; HR_v1.0 p450</div> <div>follow CheckList_1.5, DF_TV5 pu-high 2,2k only, Remove R315</div>            |                                       |               |  |       |       |               |   |   |       |   |   |     |

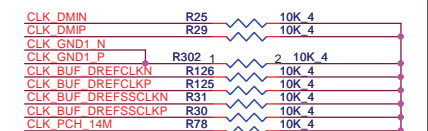


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### Stuff for Integrated CLK Gen Mode

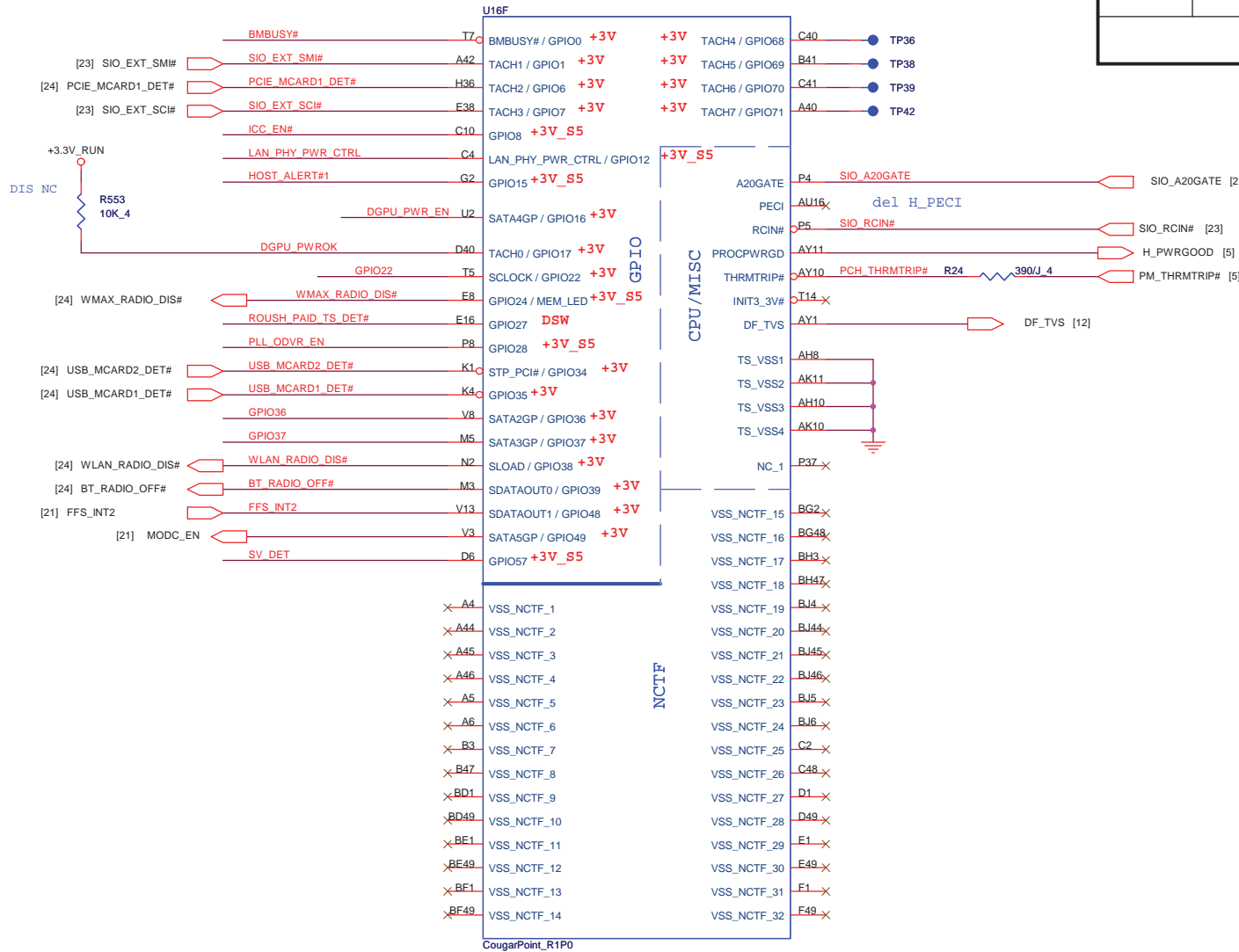


| Configurable as a GPIO or as a programmable output clock which can be configured as one of the following: |   |
|---|---|
| CLKOUTFLEX0 /GPIO064  | • 33 /27 /48/ 14.318 MHz / DC Output logic '0'  |
| CLKOUTFLEX1 /GPIO065  | unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz |
| CLKOUTFLEX2 /GPIO066  | • 33/25/27/48/24/14.318 MHz / DC Output logic '0'                                     |
| CLKOUTFLEX3 /GPIO067  | • 27/14.318 output to SIO/48/24 MHz (Default)   |



## Cougar Point (GPIO,VSS\_NCTF,RSVD)

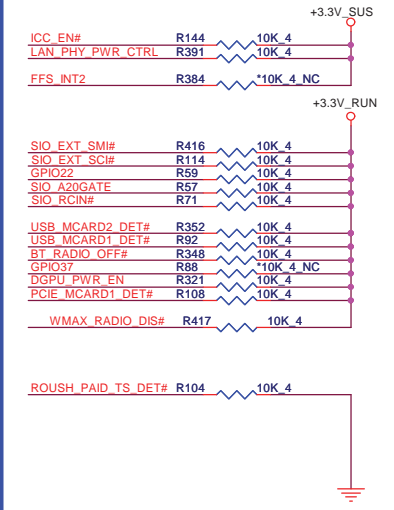
| Pin Name | Strap description            | Sampled | Configuration                       |
|----------|------------------------------|---------|-------------------------------------|
| GPIO28   | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (Default) |



Ask Intel, what's the function?

Add Description in EC GPIO table (keyboard controller reset)

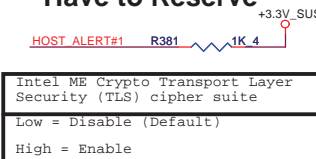
## GPIO Pull-up/Pull-down(CLG)



## Can be del



## Have to Reserve



Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

## MFG-TEST Can be del



## SGPIO Confirm with Intel



BMBUSY#:(Intel feedback)

Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:

If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3\_3.

CRB(V1.0)P28: it has 1K PU and 100 ohm pull down for validation purpose.

DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

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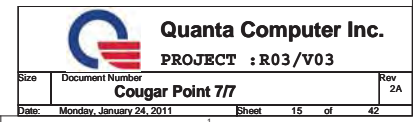
**Cougar Point 6/7**

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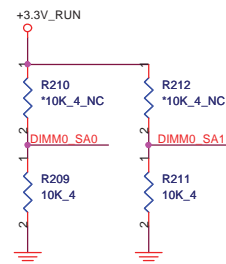
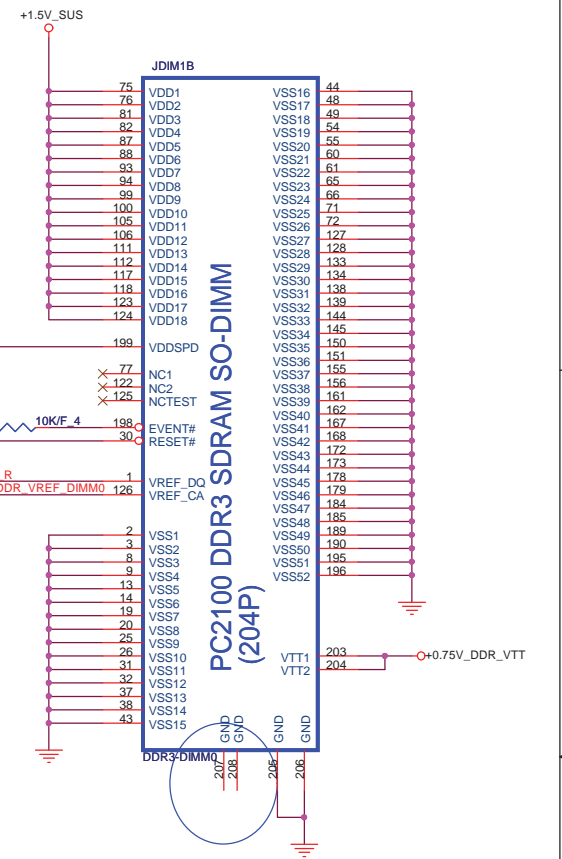
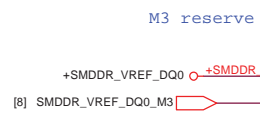
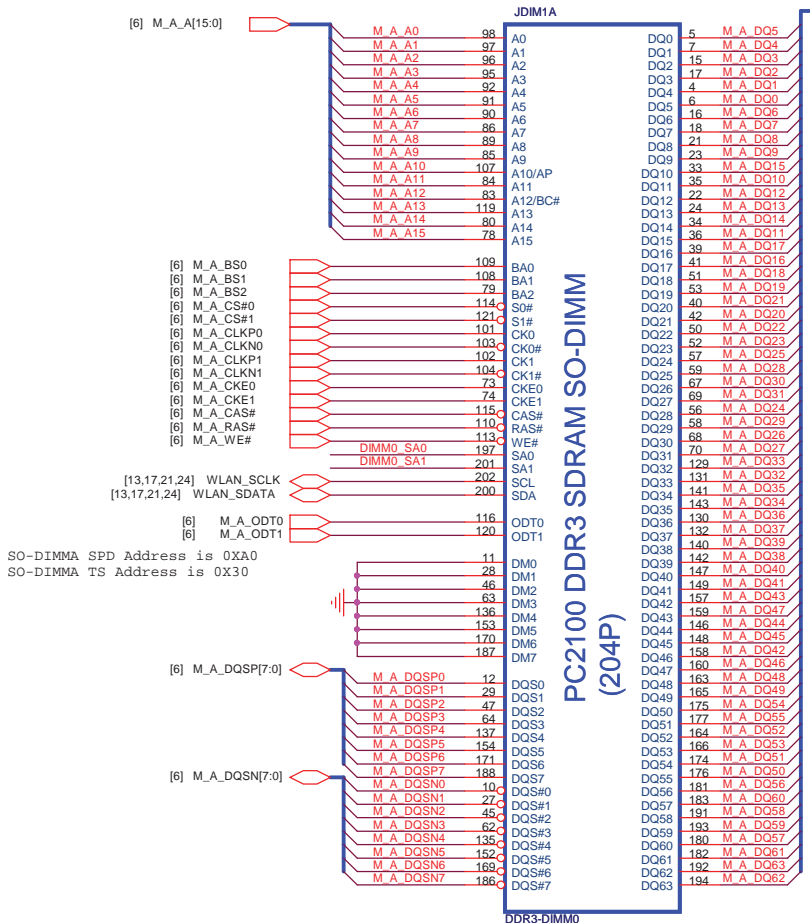
Rev 2A

Cougar Point (POWER)



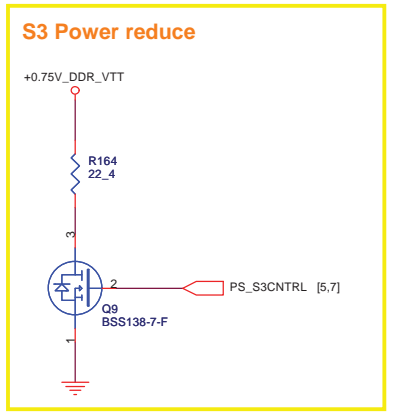
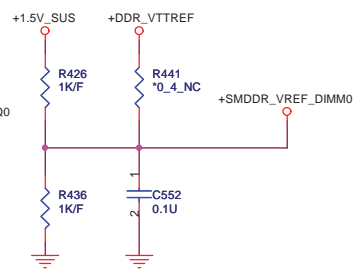
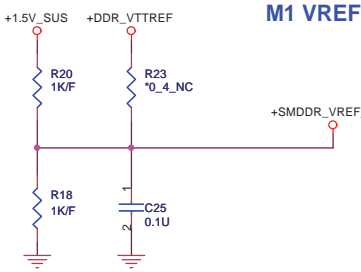
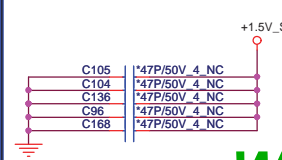
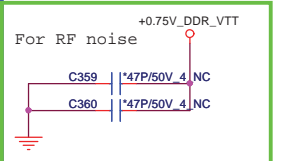
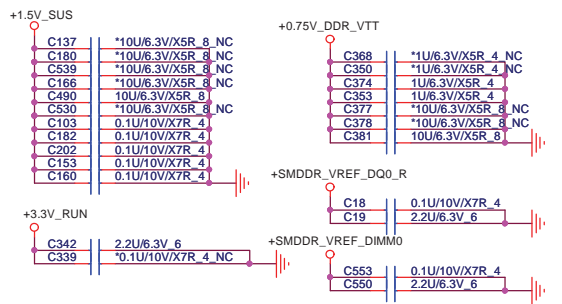


H=8.0mm,RVS

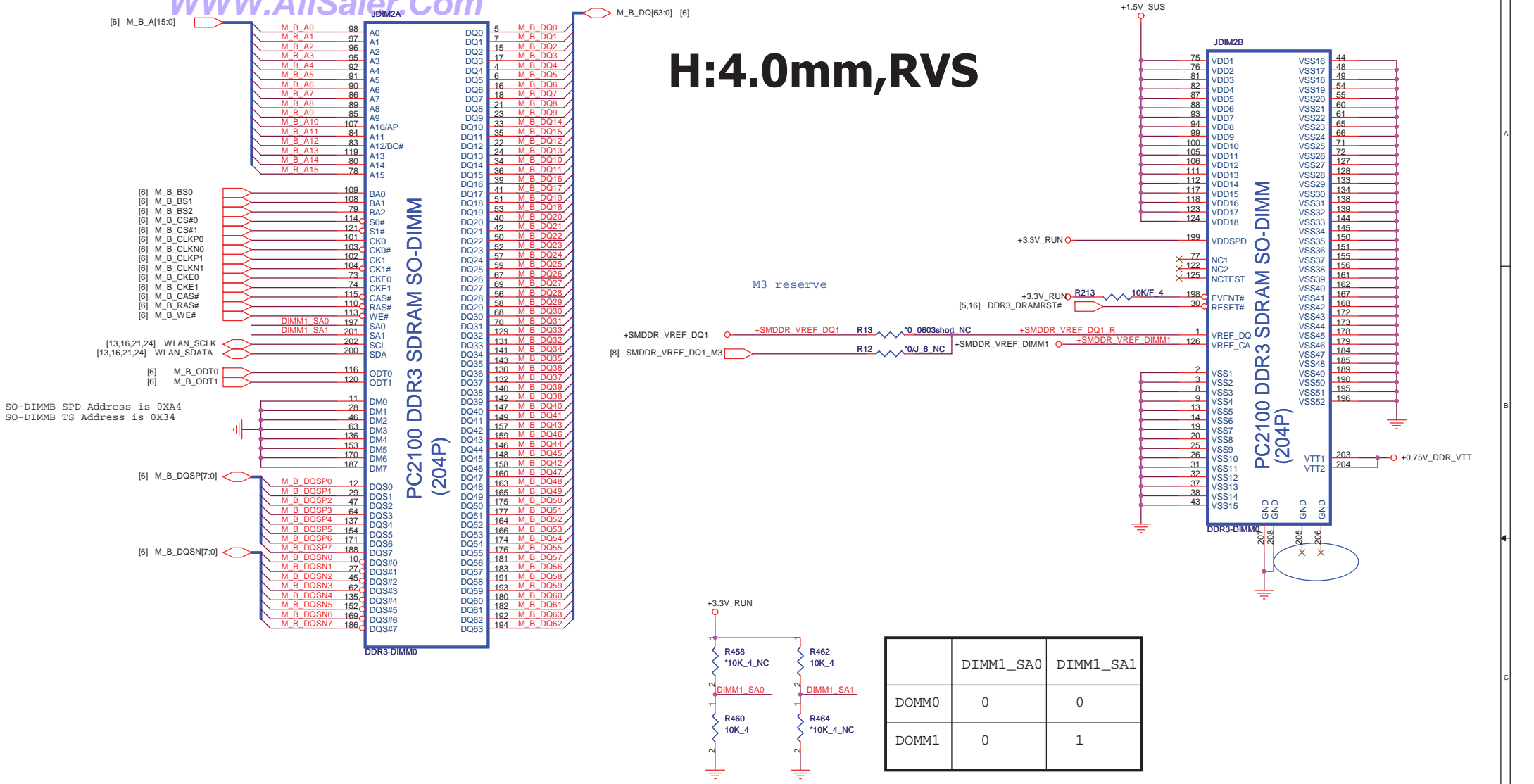


|       | DIMM0_SA0 | DIMM0_SA1 |
|-------|-----------|-----------|
| DOMM0 | 0         | 0         |
| DOMM1 | 0         | 1         |

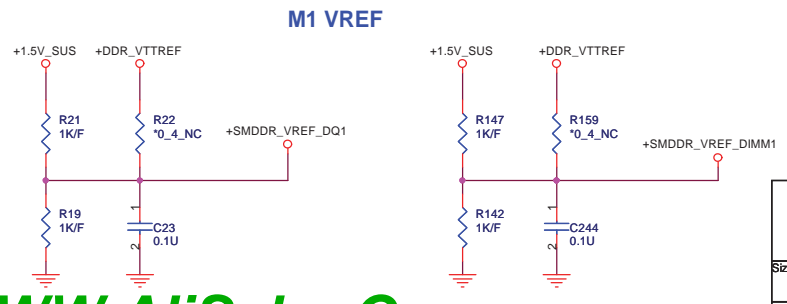
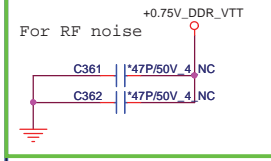
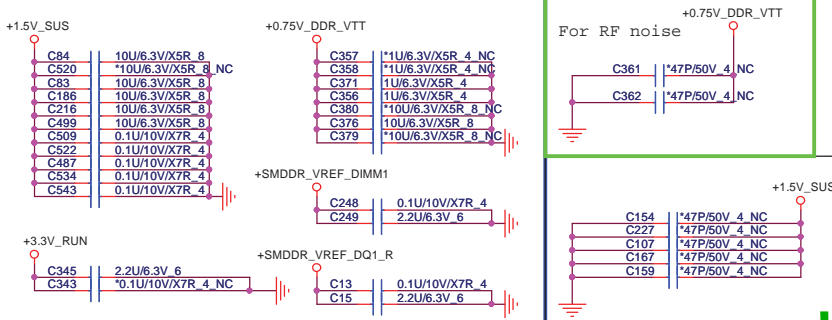
Place these Caps near So-Dimm0.

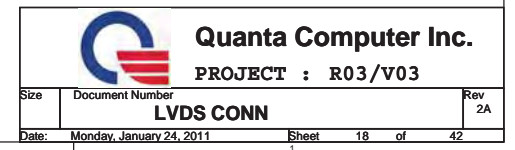


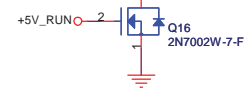
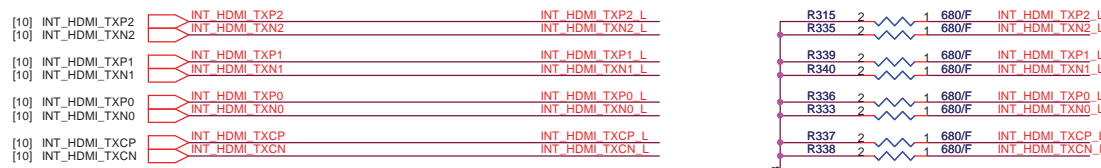
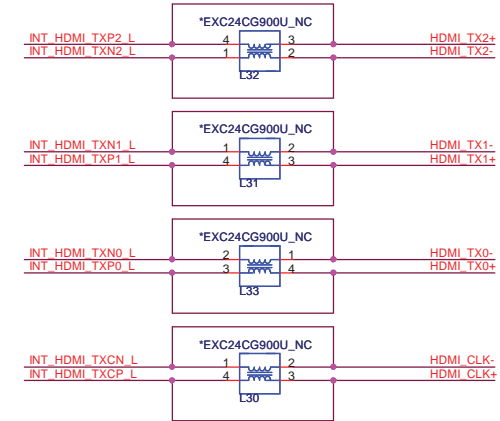
H:4.0mm,RVS



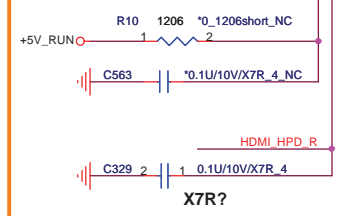
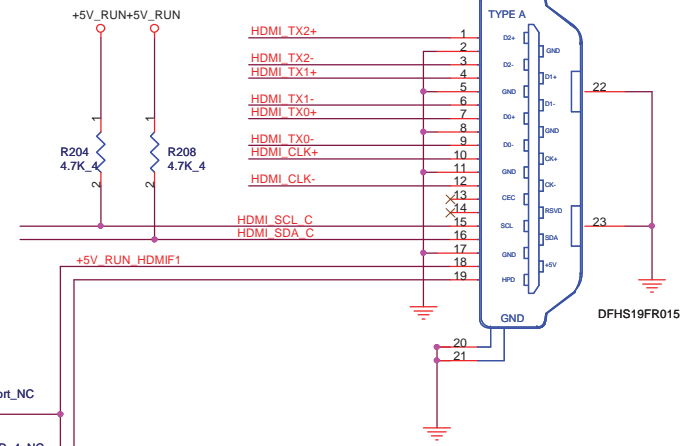
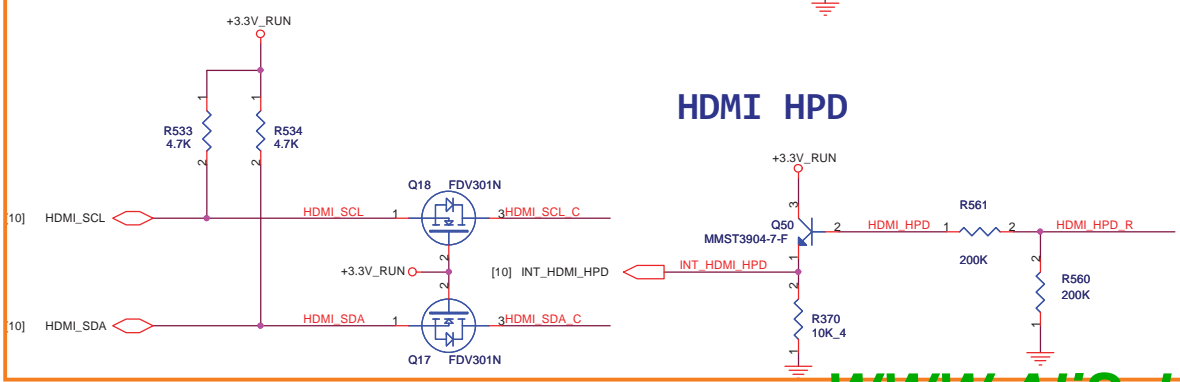
Place these Caps near So-Dimm2.





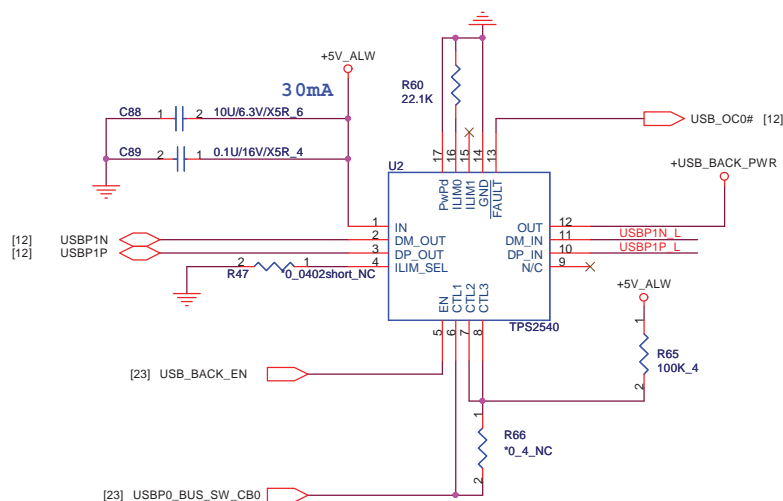


### HDMI HPD



# ESATA + USB Conn + Power share

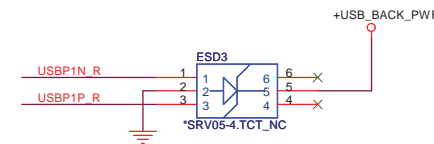
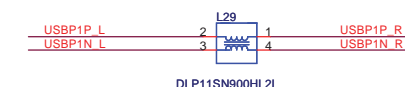
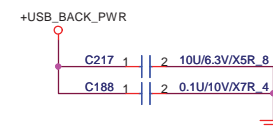
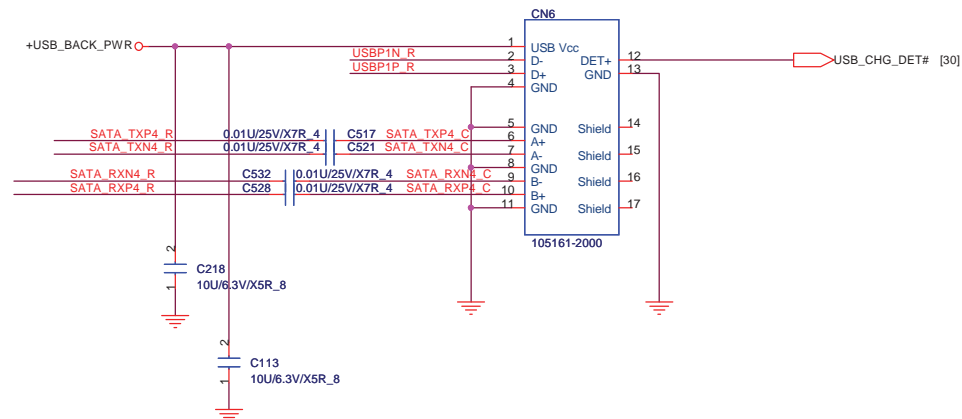
## S3/S5 USB charging circuit



| USBP0_BUS_SW_CB0 | Mode             |
|------------------|------------------|
| Low              | DCP, Auto-detect |
| High             | CDP, BC Spec 1.1 |

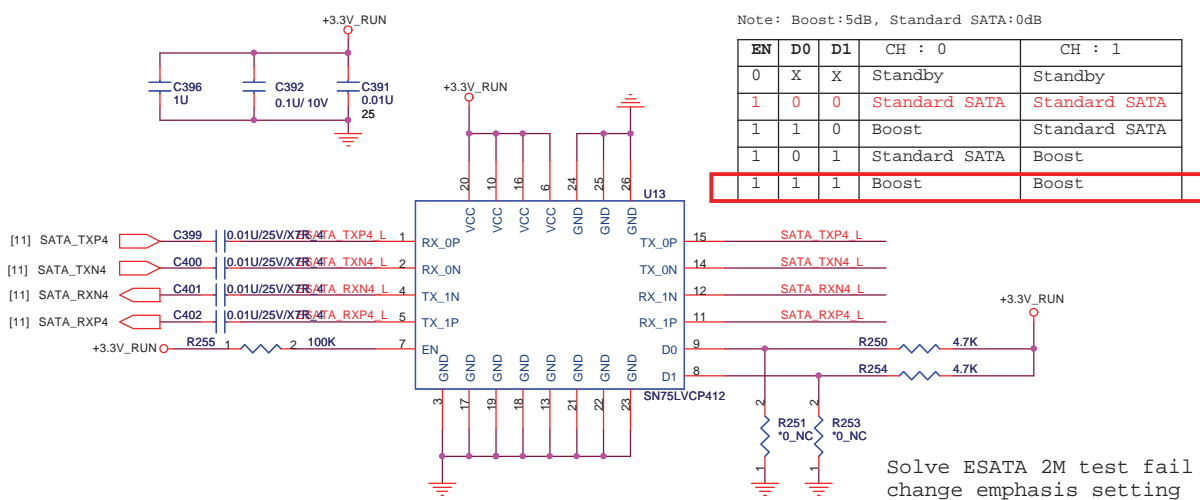
ES(PG1.0): Stuff R66, Remove R65  
MP(PG1.1): Remove R66, Stuff R65

|               | R8224     | mA          |
|---------------|-----------|-------------|
| OC limitation | 100k ohm  | 480         |
|               | 22.1k ohm | 2171        |
|               |           | Applied Now |



## E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB

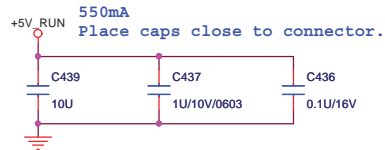
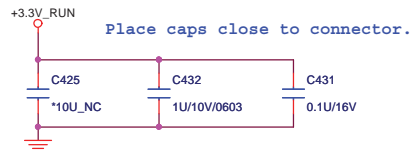
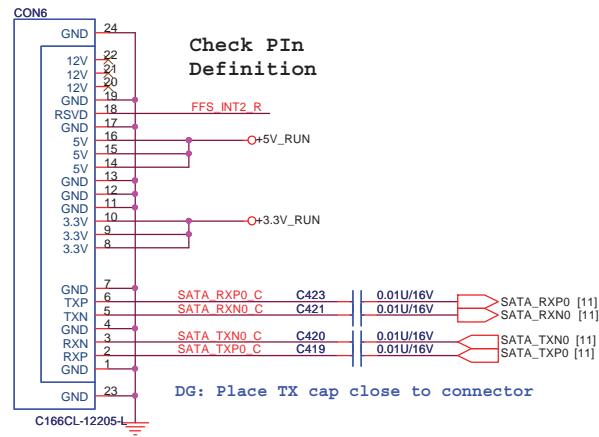


Note: Boost:5dB, Standard SATA:0dB

| EN | D0 | D1 | CH : 0        | CH : 1        |
|----|----|----|---------------|---------------|
| 0  | X  | X  | Standby       | Standby       |
| 1  | 0  | 0  | Standard SATA | Standard SATA |
| 1  | 1  | 0  | Boost         | Standard SATA |
| 1  | 0  | 1  | Standard SATA | Boost         |
| 1  | 1  | 1  | Boost         | Boost         |

Solve ESATA 2M test fail issue,  
change emphasis setting

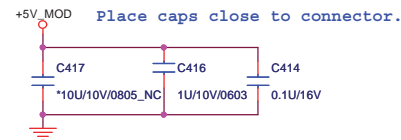
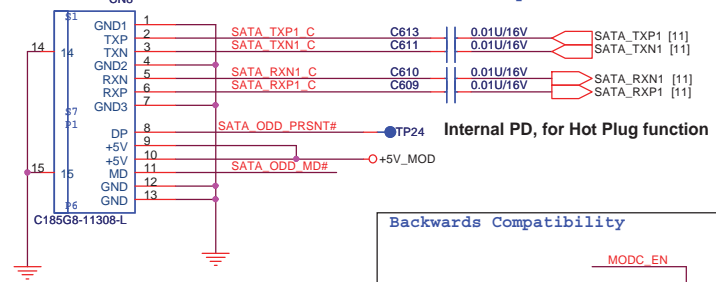
## SATA Connector UM8



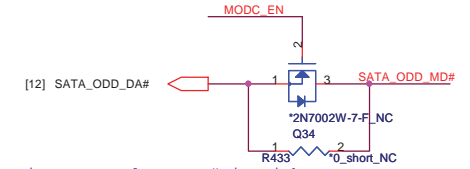
## ODD Connector

Change connector as ME request

DG: Place TX cap close to connector



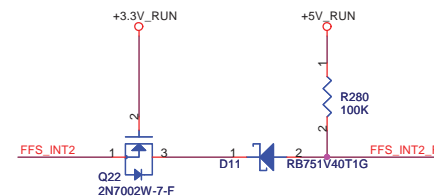
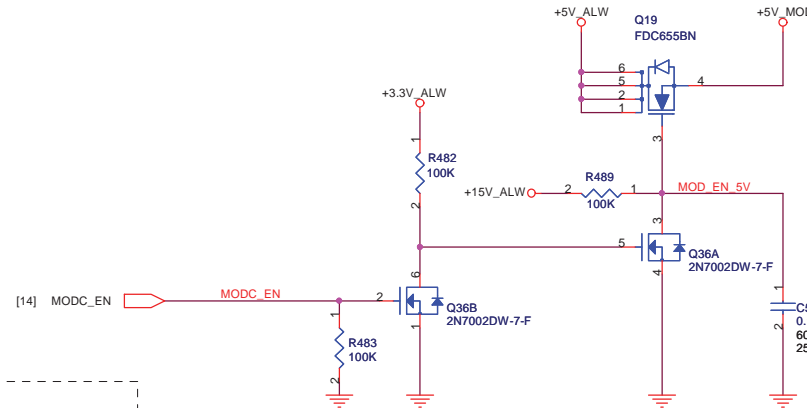
### Backwards Compatibility



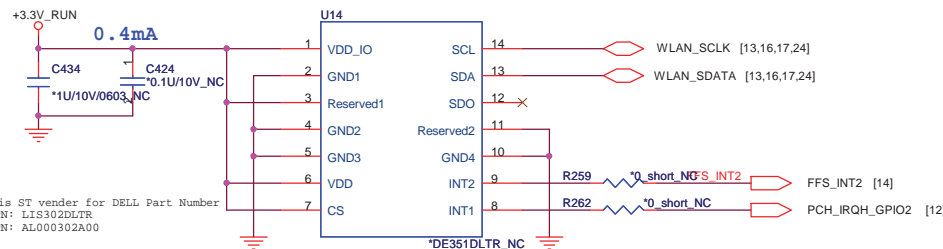
Drive powered on, MD# is High  
Drive powered off, MD# is Low

Because the drive does not support ZPODD, the driver never powers off the power FET and never connects the MD/DA pin to the drive

change RUN to ALW, change TRANS MOS for cost down



### 3-axis Fall Sensor (HDD data protector)



DE351DL is ST vender for DELL Part Number  
Vender PN: LIS302DLTR  
Quanta PN: AL000302A00

From FM9

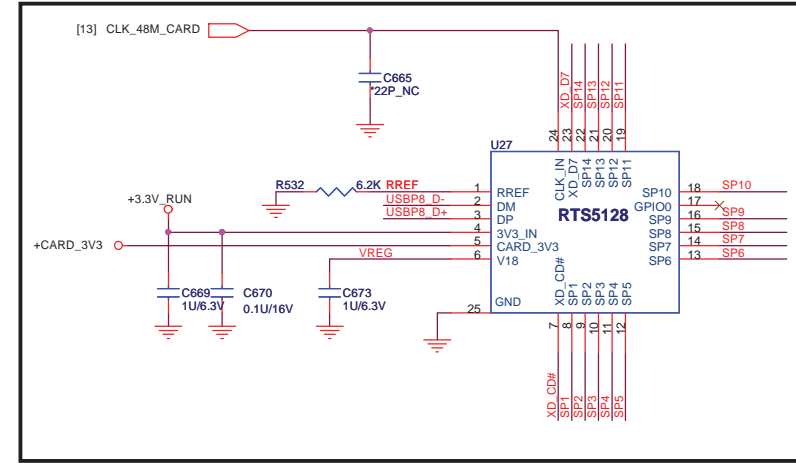
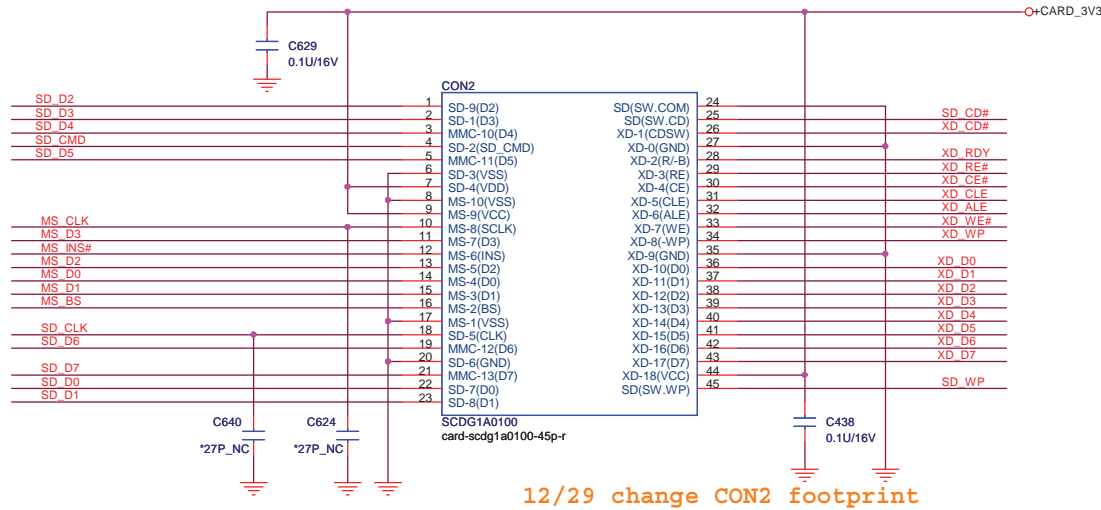


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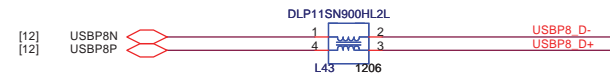
| Size                           | Document Number | Rev |
|--------------------------------|-----------------|-----|
|                                | SATA HDD/ODD    | 2A  |
| Date: Monday, January 24, 2011 | Sheet 21 of 42  |     |

## RTS5128-QFN24

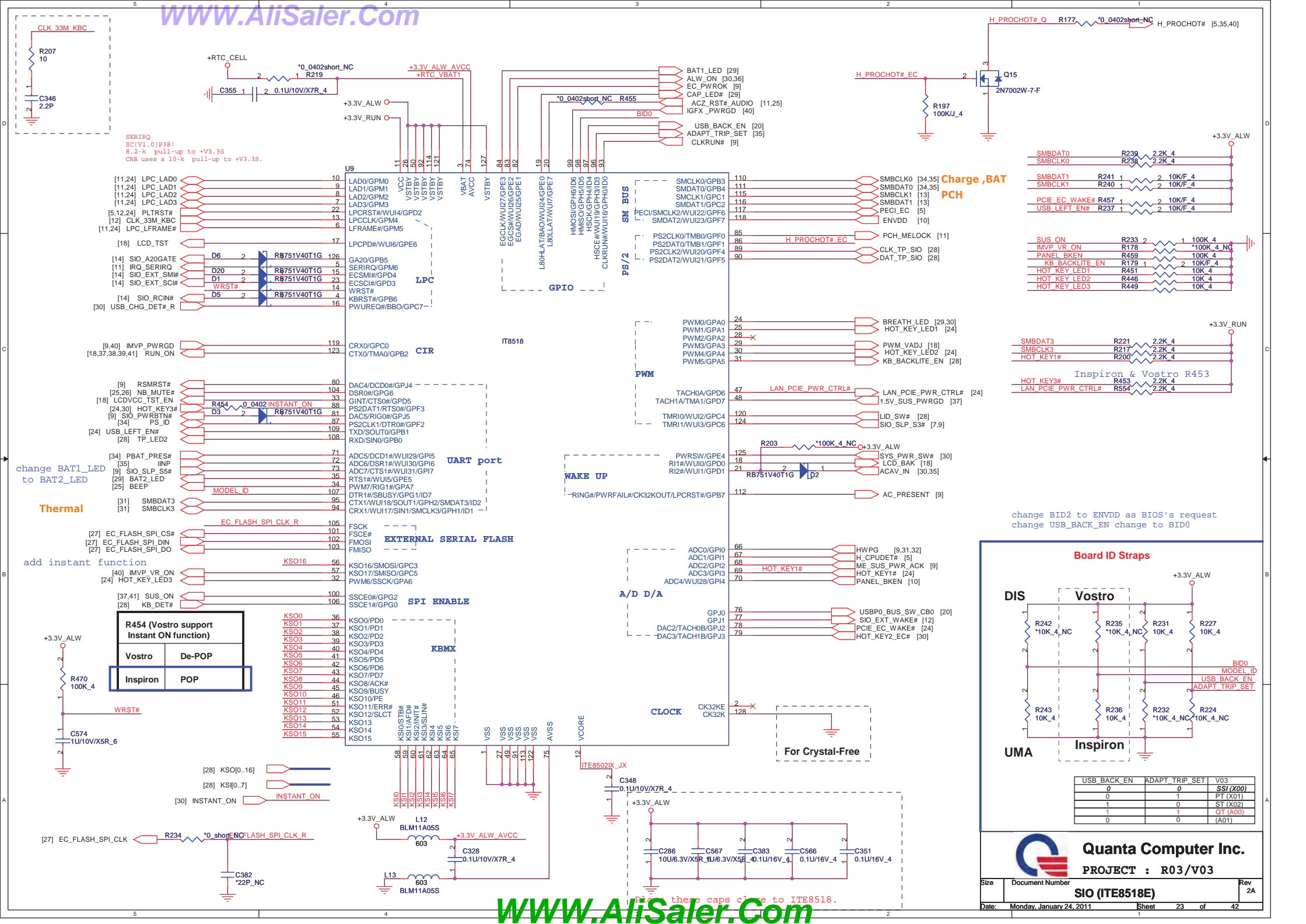


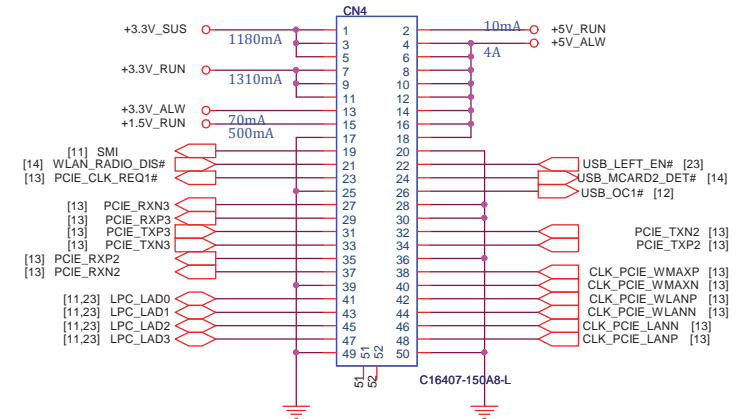
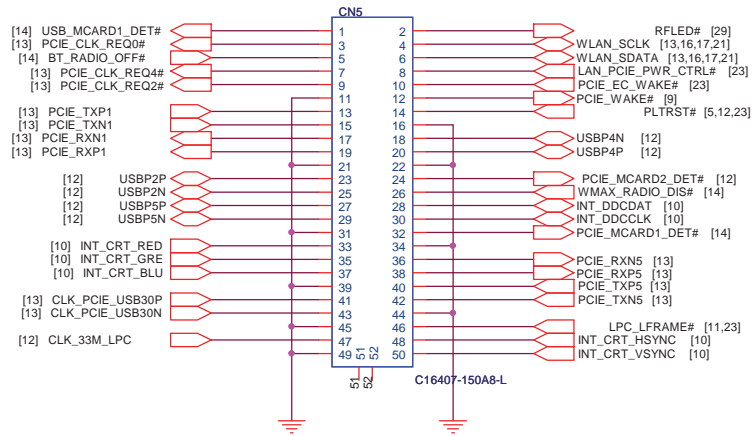
|      |        |        |         |
|------|--------|--------|---------|
| SP1  | XD_RDY | SD_WP  | MS_CLK  |
| SP2  | XD_RE# | SD_D1  | MS_INS# |
| SP3  | XD_CE# | SD_D0  | MS_D7   |
| SP4  | XD_CLE | SD_D7  | MS_D3   |
| SP5  | XD_ALE | SD_D6  | MS_D6   |
| SP6  | XD_WE# | SD_CD# | MS_D0   |
| SP7  | XD_WP  | SD_CLK | MS_D2   |
| SP8  | XD_D0  | SD_D5  | MS_D0   |
| SP9  | XD_D1  | SD_CMD | MS_D4   |
| SP10 | XD_D2  | SD_D4  | MS_D1   |
| SP11 | XD_D3  | SD_D2  | MS_D5   |
| SP12 | XD_D4  | SD_D3  | MS_BS   |
| SP13 | XD_D5  | SD_D1  |         |
| SP14 | XD_D6  | SD_D0  |         |

Share Pin

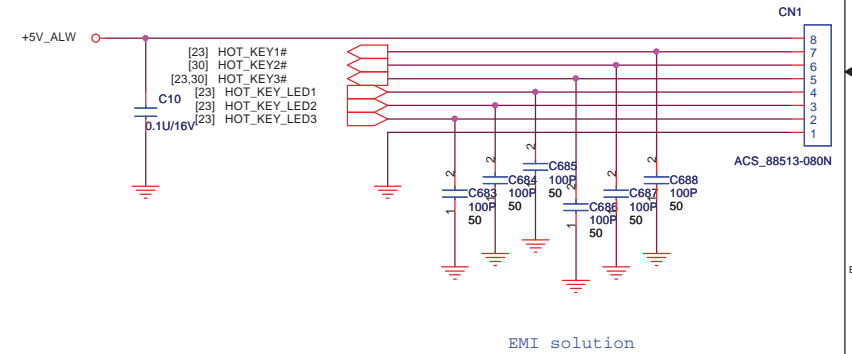




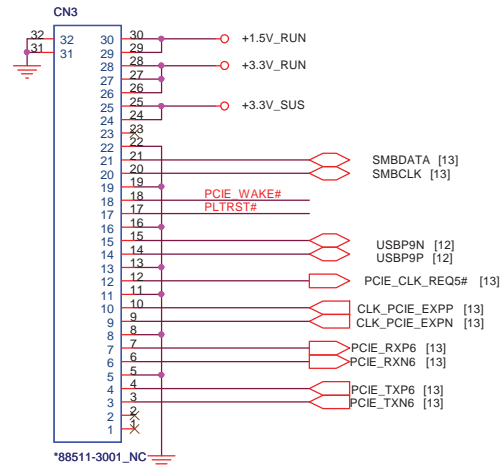




## HOTKEY CON



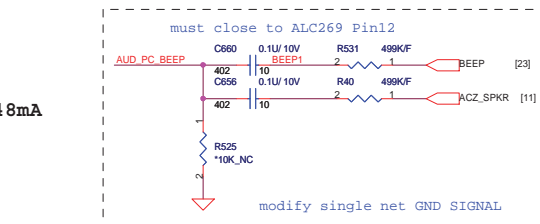
## MB to Express Card Board



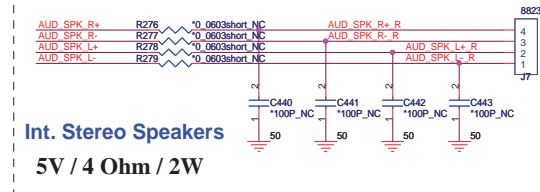
**Quanta Computer Inc.**  
PROJECT : R03/V03

VA type: PIN28 作為MIC之偏壓  
PIN31接A-GND

VB type: PIN31 作為MIC之偏壓  
PIN28接CAP作為內部LDO  
output 輸出濾波用



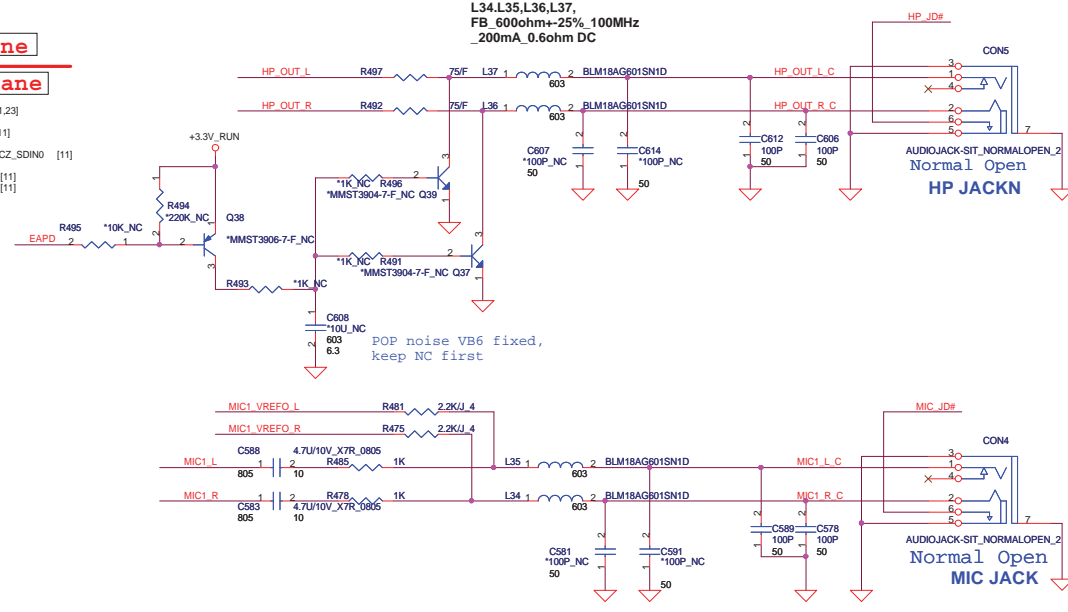
Trace width >= 40mil, Trace length < 20cm




### Int. Stereo Speakers

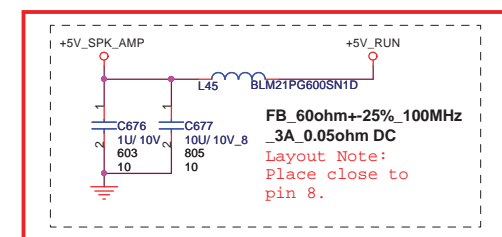
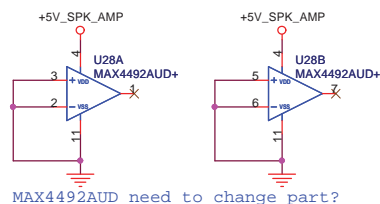
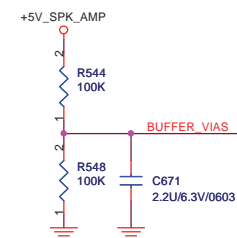
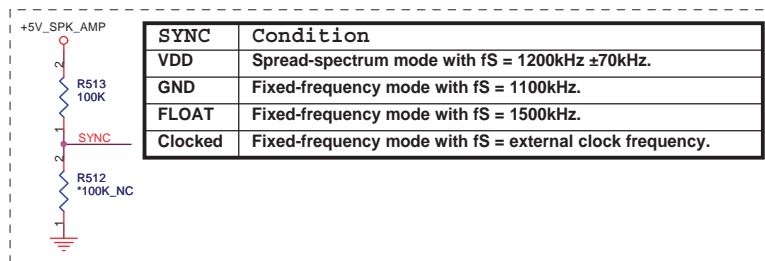
**5V / 4 Ohm / 2W**

L34.L35,L36,L37,  
FB\_600ohm+-25%\_100MHz  
200mA 0.6ohm DC

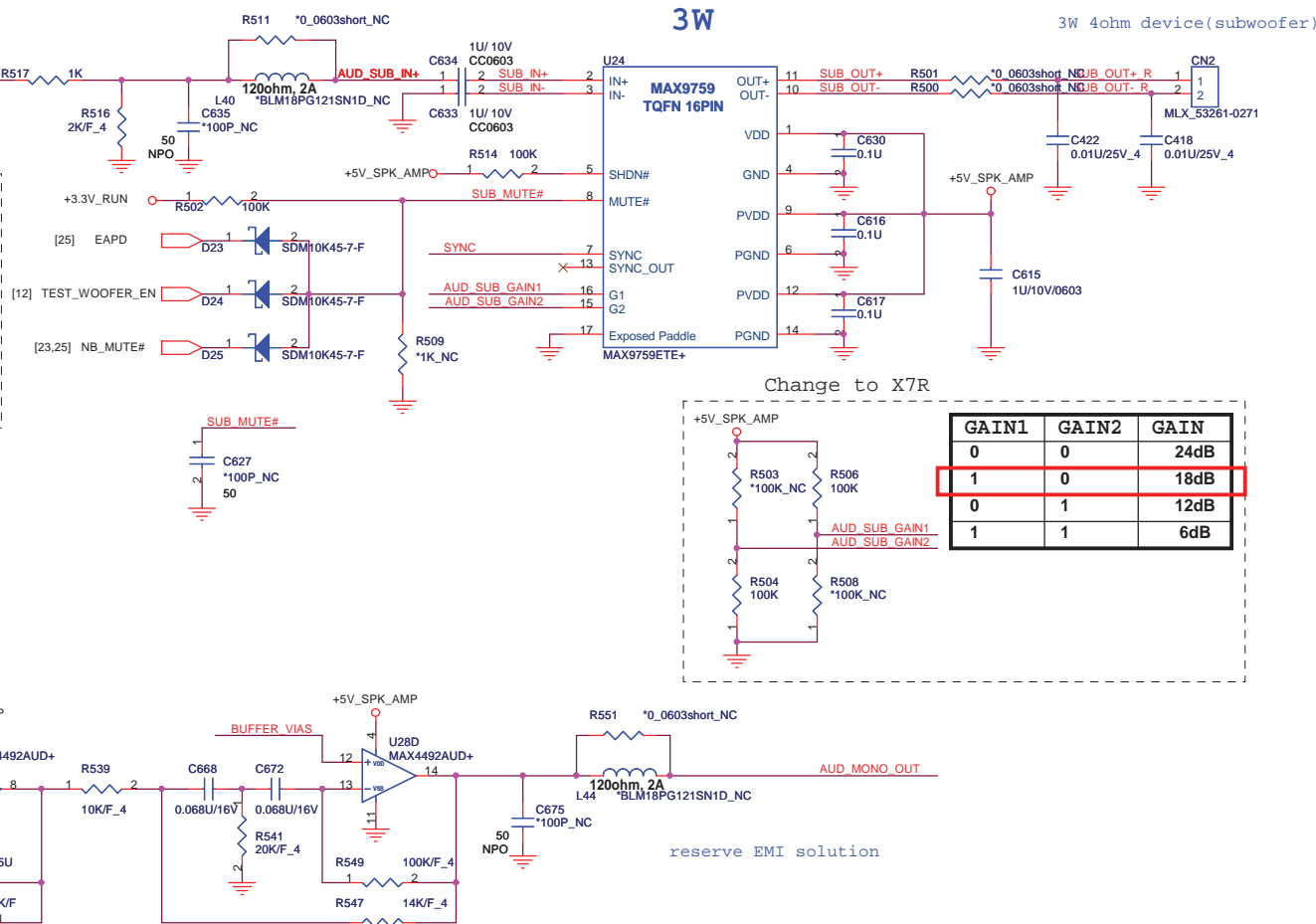


|   |                          |                |
|---|--------------------------|----------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : R03/V03</b> |                          |                |
| Size  | Document Number          | Rev            |
|   | <b>Azelia CODEC</b>      | <b>2A</b>      |
| Date:   | Monday, January 24, 2011 | Sheet 25 of 42 |

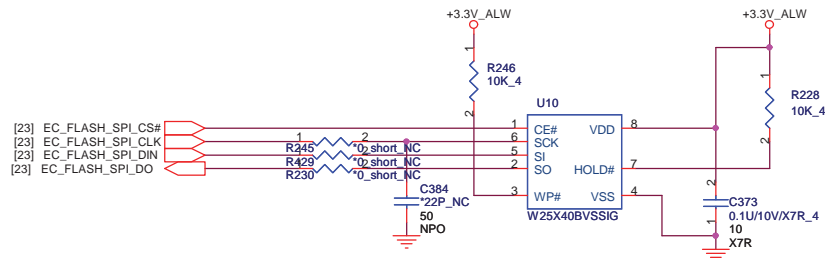
# INTERNAL SUBWOOFER AMP Only for 17''



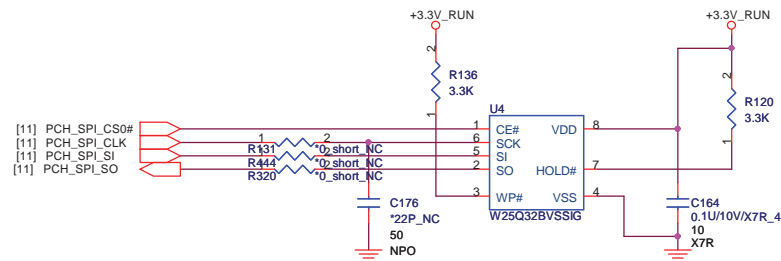
place close to connector side



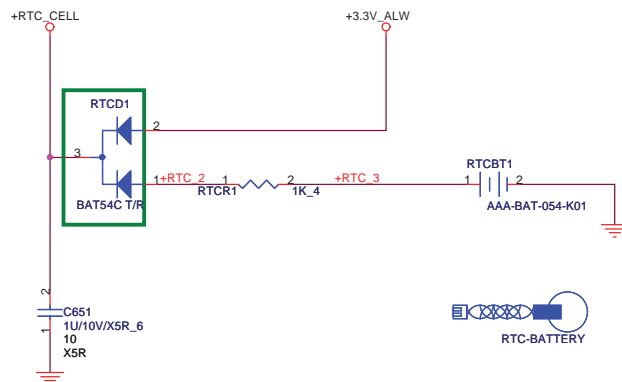
## For EC 4Mbit (512K Byte)



## For PCH 32Mbit (4M Byte)



## RTC



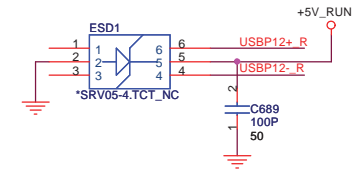
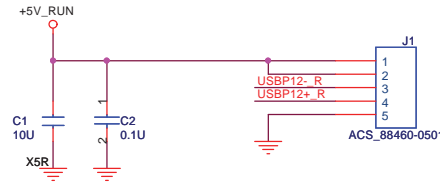
Double, 25°C, Vf=0.4V, If=25mA  
one, 25°C, Vf=0.35V, If=15.8mA

james command change part number

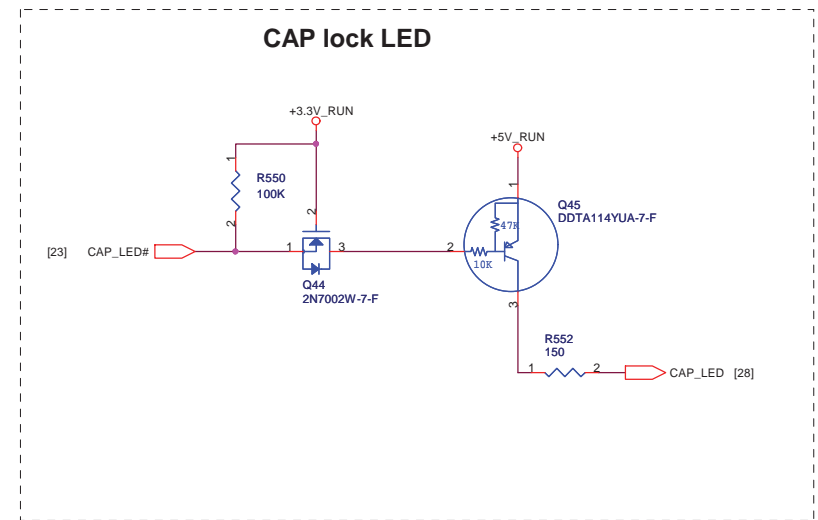
## Touch Screen Module

Note:

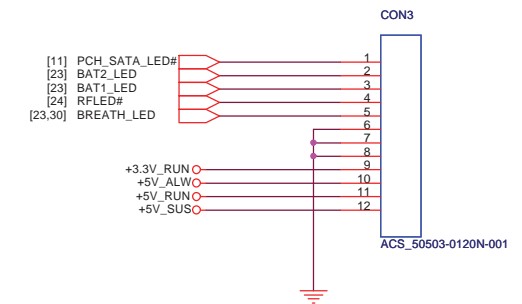
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.







### MB to LED Board conn

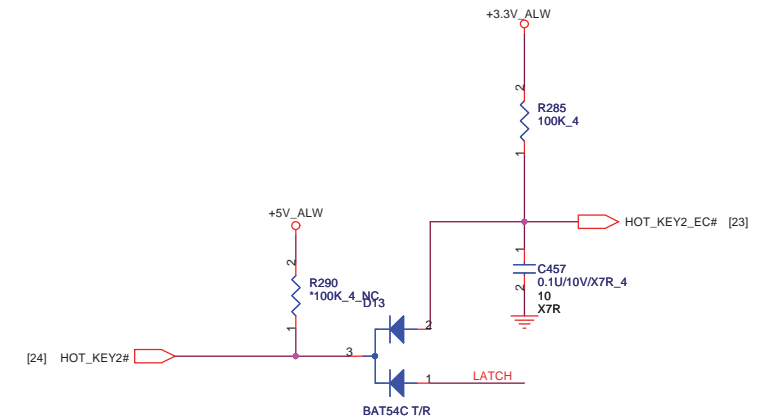
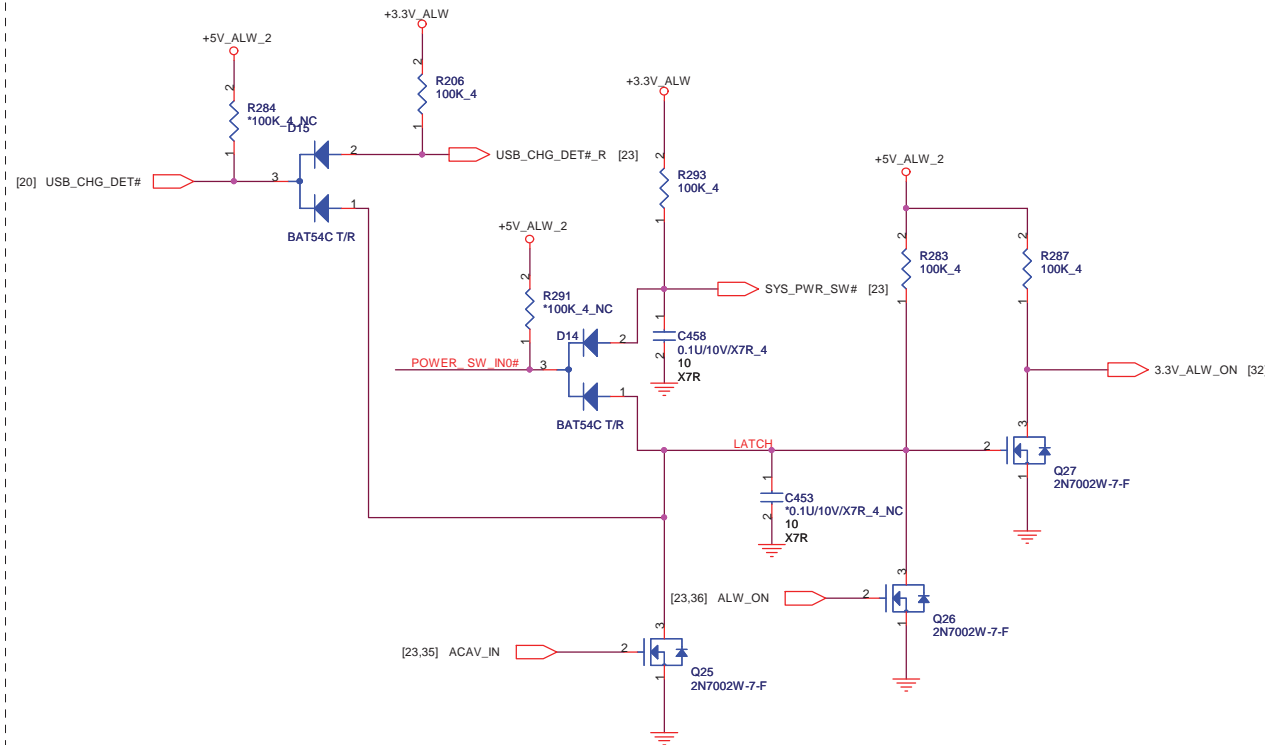


**Quanta Computer Inc.**  
**PROJECT : R03/V03**

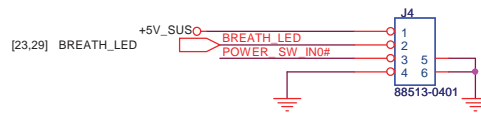
|       |                          |                |
|-------|--------------------------|----------------|
| Size  | Document Number          | Rev            |
|       | <b>LED</b>               | 2A             |
| Date: | Monday, January 24, 2011 | Sheet 29 of 42 |



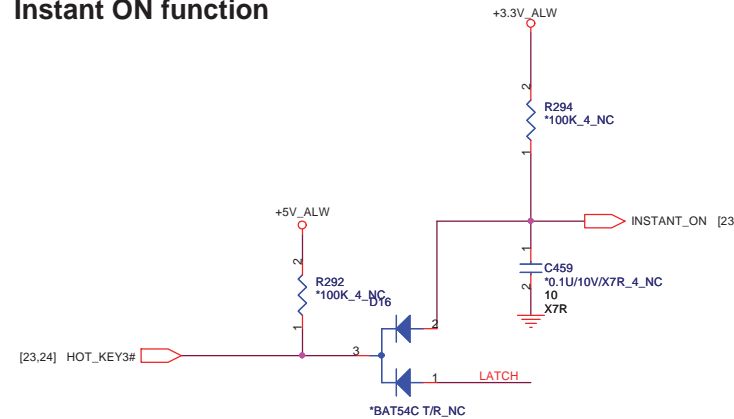
## 3VALW ON POWER LOGIC



## PWR button board form UM7



## Instant ON function



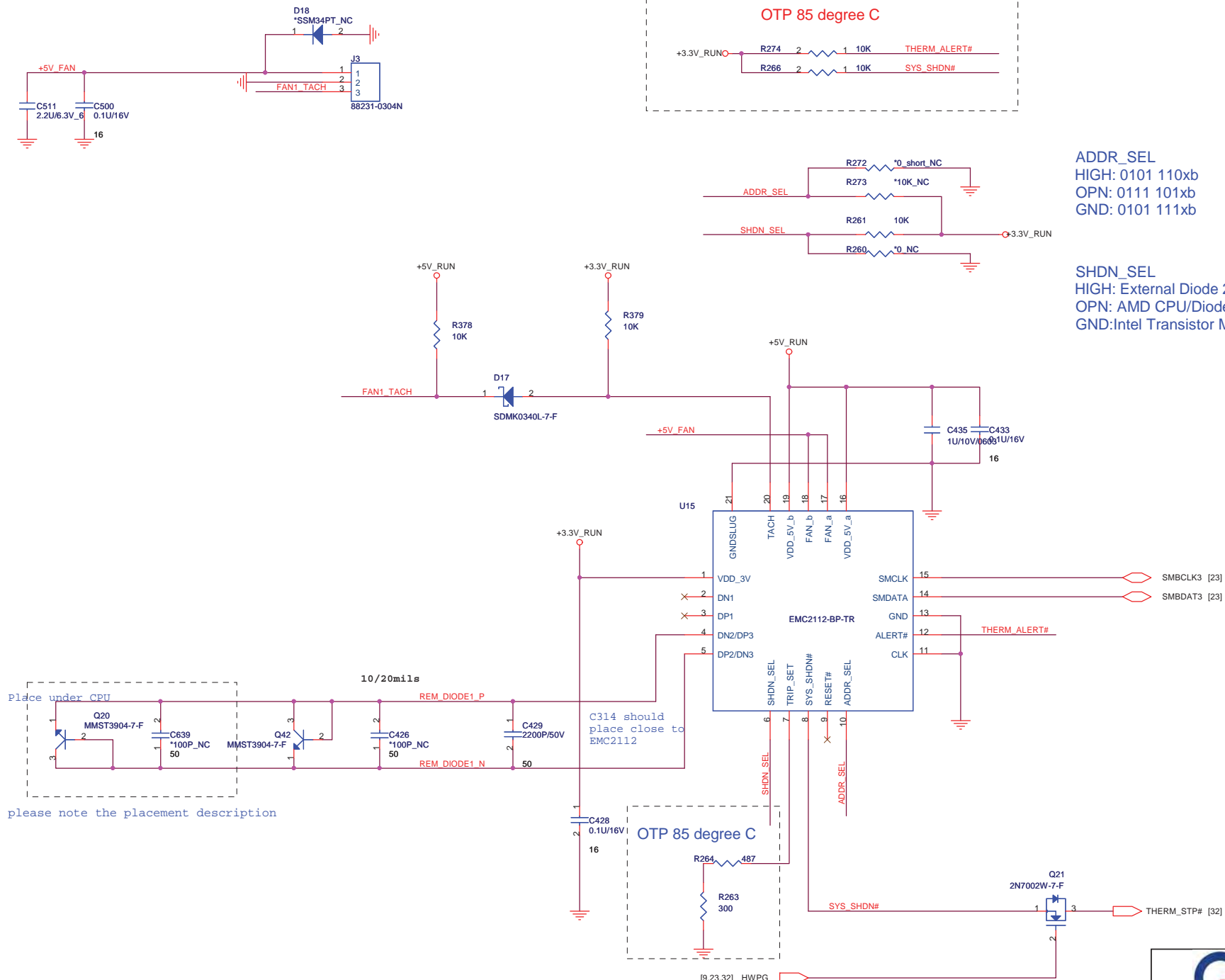
Quanta Computer Inc.

PROJECT : R03/V03

| Size  | Document Number          | Rev            |
|-------|--------------------------|----------------|
|       | PWR SW/LED               | 2A             |
| Date: | Monday, January 24, 2011 | Sheet 30 of 42 |


# FAN CONTROL

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ADDR\_SEL  
HIGH: 0101 110xb  
OPN: 0111 101xb  
GND: 0101 111xb

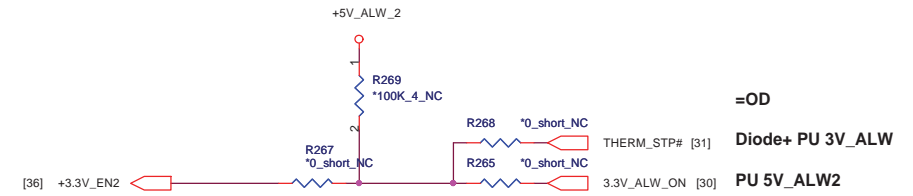
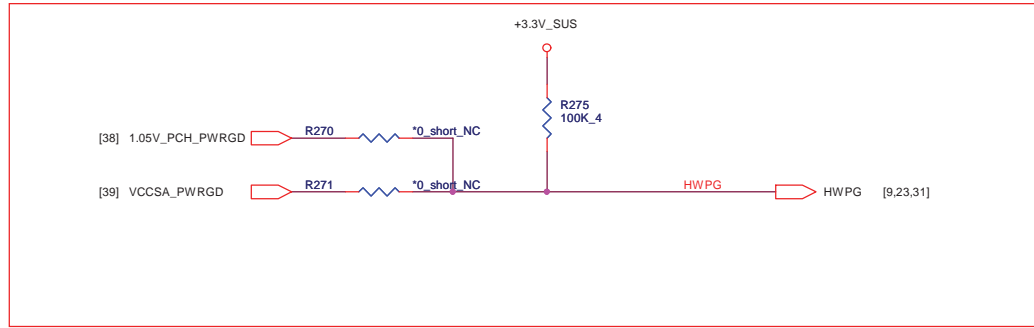
SHDN\_SEL  
HIGH: External Diode 2 Mode  
OPN: AMD CPU/Diode Mode  
GND: Intel Transistor Mode

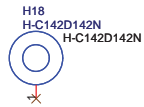
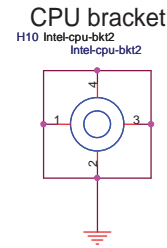
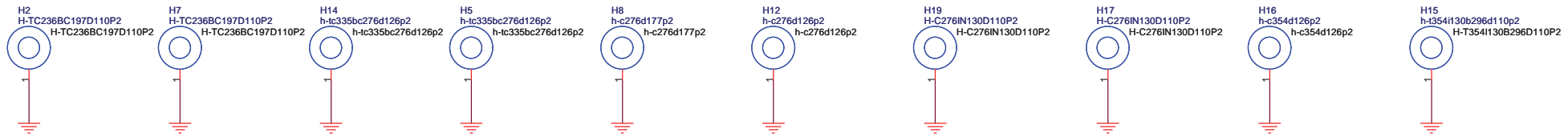


**Quanta Computer Inc.**  
**PROJECT : R03/V03**

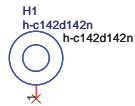
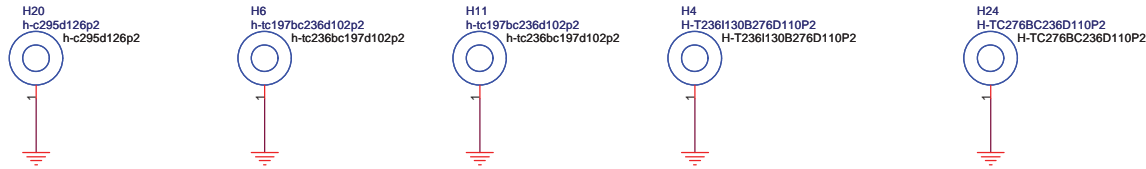
|                          |                          |                |
|--------------------------|--------------------------|----------------|
| Size                     | Document Number          | Rev            |
| <b>FAN &amp; THERMAL</b> |                          | 2A             |
| Date:                    | Monday, January 24, 2011 | Sheet 31 of 42 |

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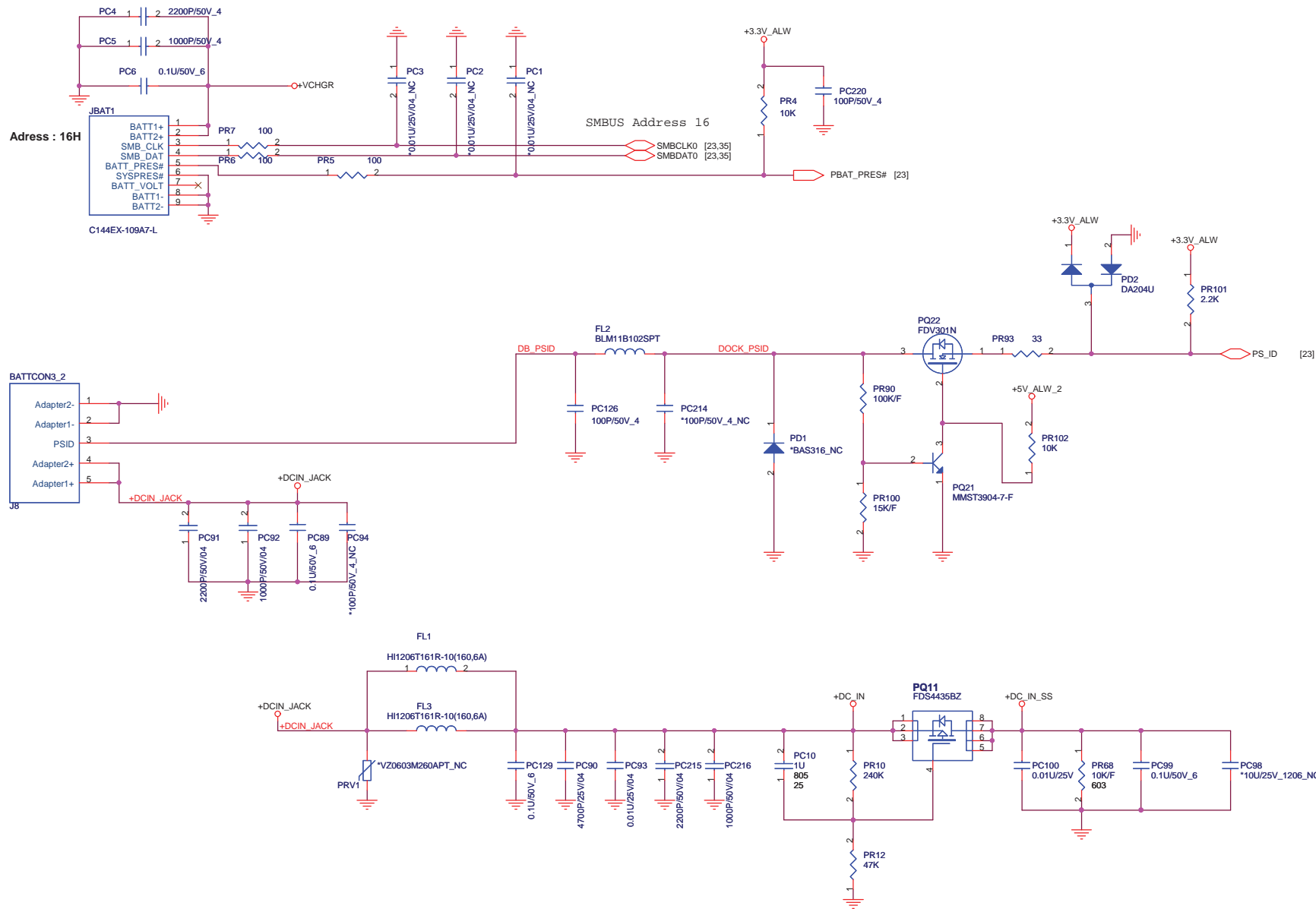
H6, H11 on the button side

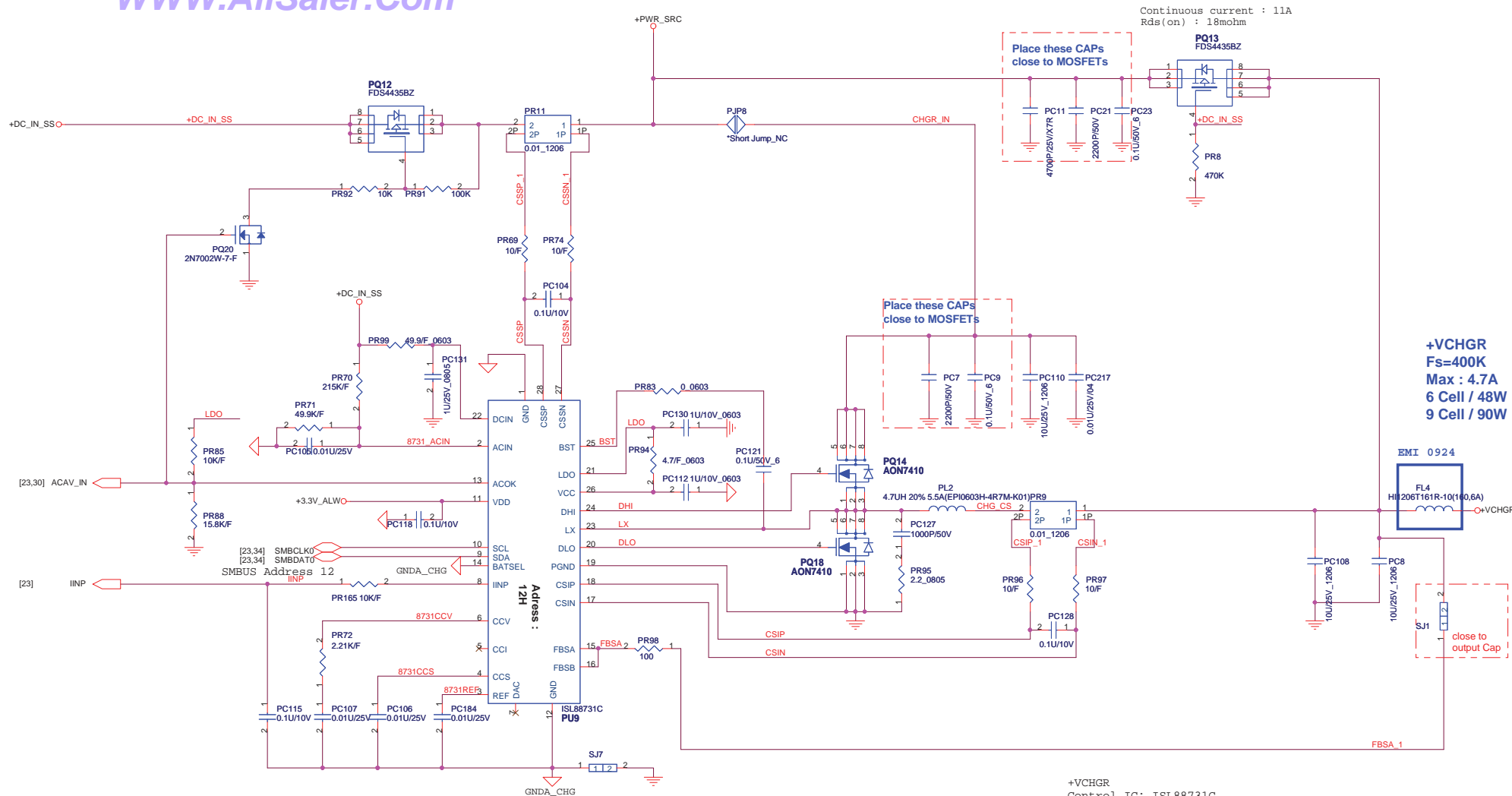


**Quanta Computer Inc.**  
**PROJECT : R03/V03**

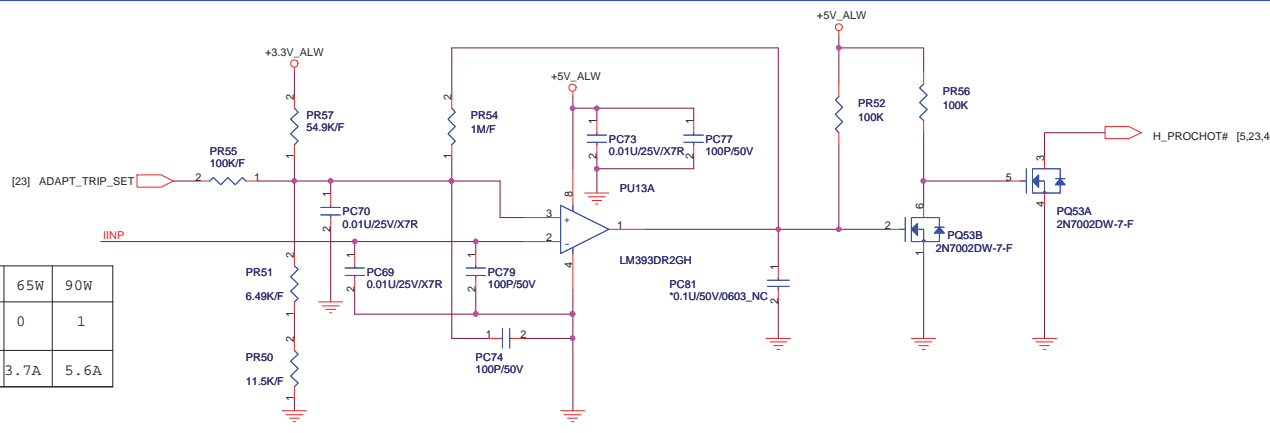
| Size  | Document Number          | Rev            |
|-------|--------------------------|----------------|
|       |                          | 2A             |
| Date: | Monday, January 24, 2011 | Sheet 33 of 42 |

**SCREW PAD**

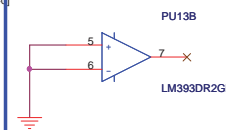




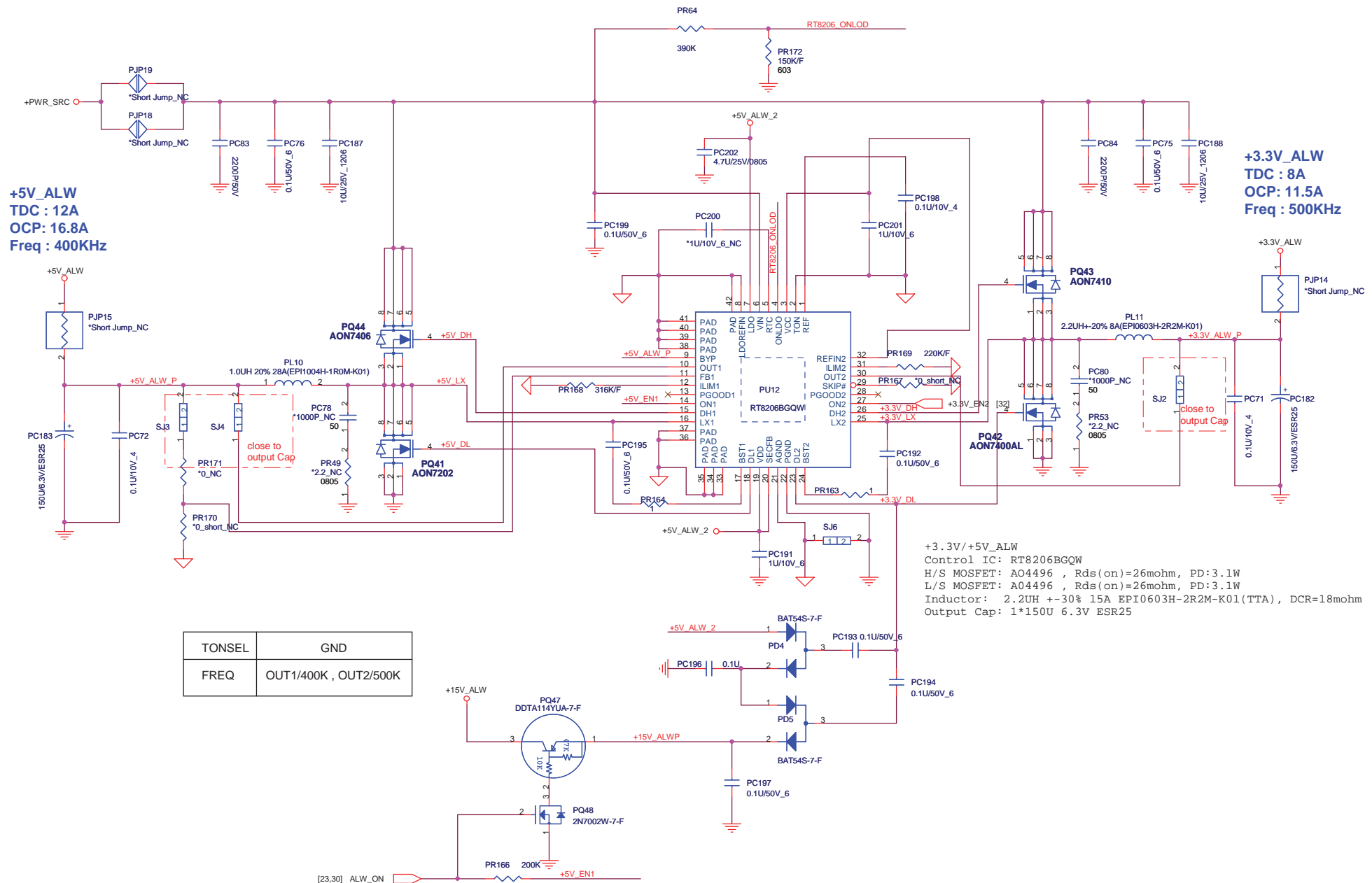
+VCHGR  
Control IC: ISL88731C  
H/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W  
L/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W  
Inductor: 5.8uH +-30% 5.5A SDSLL10D40F-5R8Y(TTA), DCR=22mohm  
Output Cap: 2\*10U 25V(+/-10%,X6S,1206)



|                 |      |      |
|-----------------|------|------|
| Adapter type    | 65W  | 90W  |
| ADAPT_TRIP_SET  | 0    | 1    |
| SETTING CURRENT | 3.7A | 5.6A |



DC/DC +3V\_ALW/+5V\_ALW /+15V\_ALW



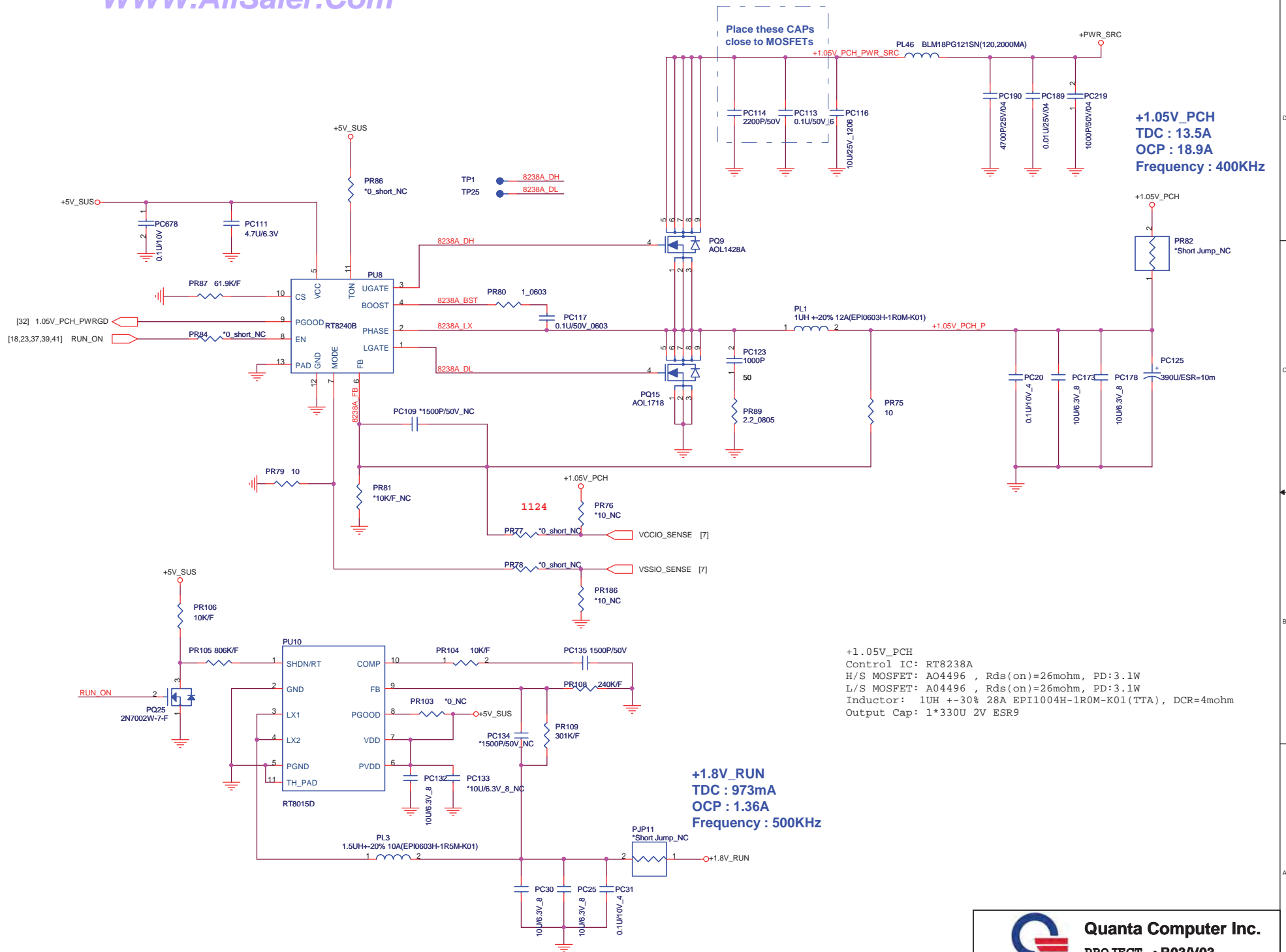


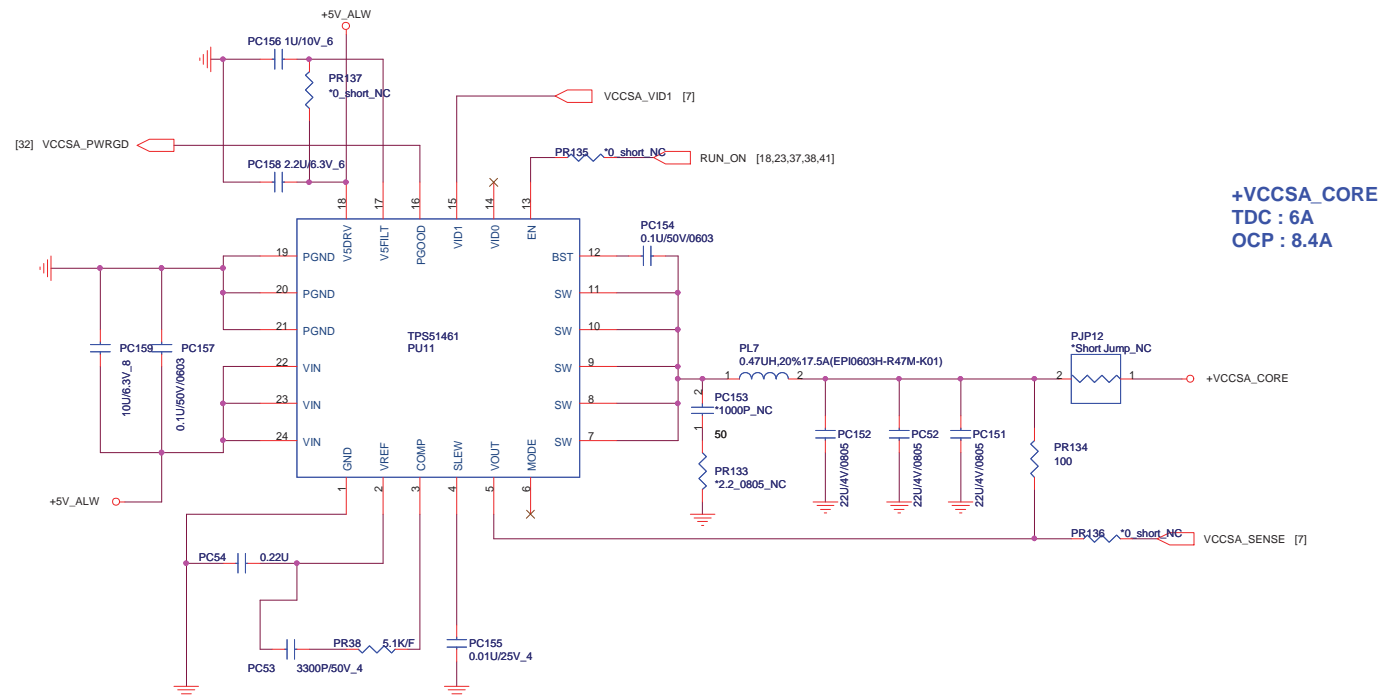


VDDQ output voltage selection

## Outputs Management by S3, S5 control

| State | S3 | S5 | VDDQ           | VTTREF          | VTT             |
|-------|----|----|----------------|-----------------|-----------------|
| S0    | HI | HI | On             | On              | On              |
| S3    | LO | HI | On             | On              | Off (Hi-Z)      |
| S4/S5 | LO | LO | On (discharge) | Off (discharge) | Off (discharge) |





|        |            |
|--------|------------|
| +VCCSA | VCCSA_VID1 |
| 0.8V   | High       |
| 0.9V   | Low        |



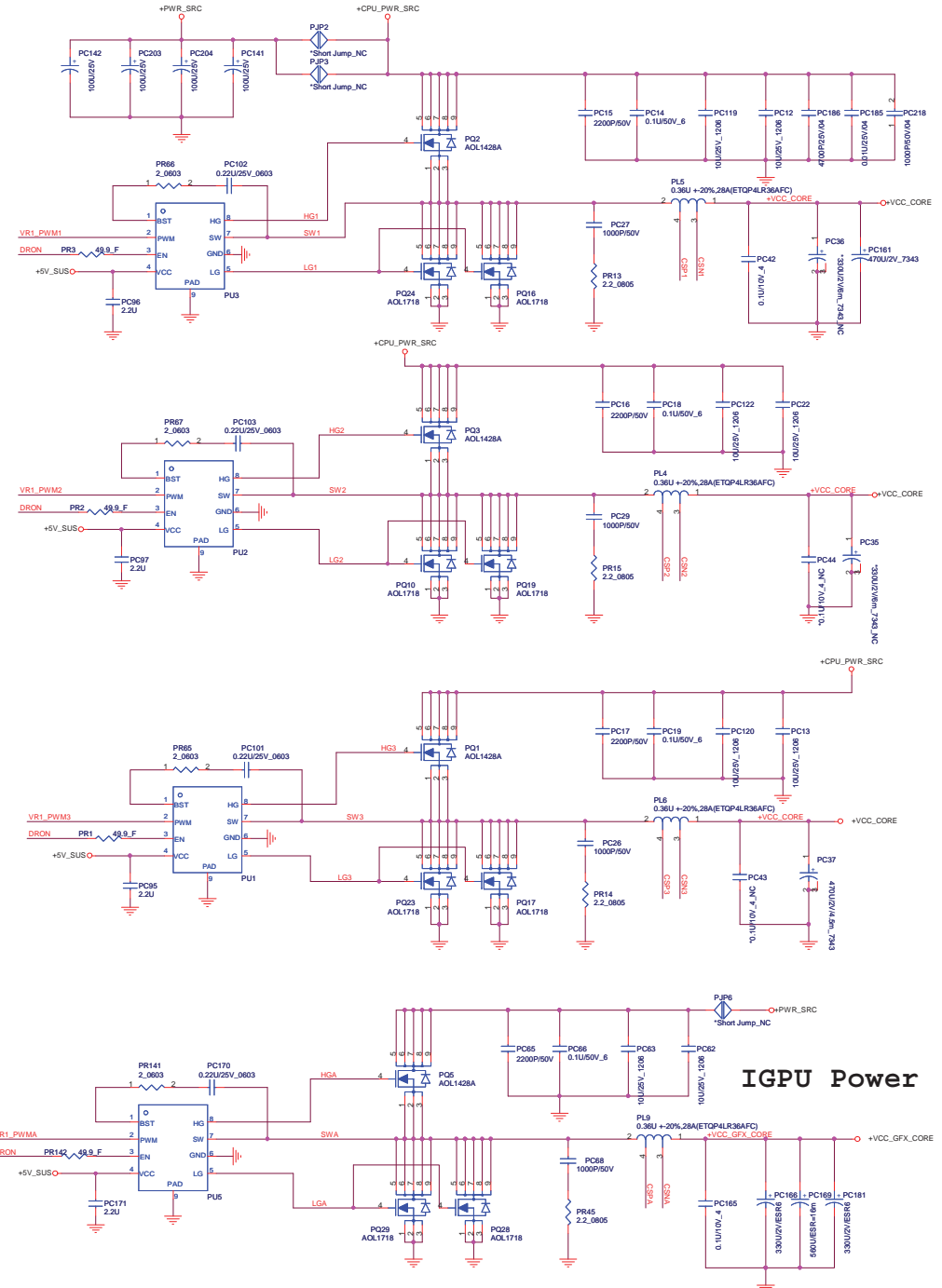
Quanta Computer Inc.


PROJECT : R03/V03

VCCSA (TPS51461)

|      |                 |     |
|------|-----------------|-----|
| Size | Document Number | Rev |
|      |                 | 2A  |

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|   |                          |                |
|---|--------------------------|----------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : R03/V03</b> |                          | Rev            |
| Size  | Document Number          | 2              |
| <b>+VCC_CORE (NCP6131S)</b>   |                          |                |
| Date:   | Monday, January 24, 2011 | Sheet 40 of 42 |

